

1174

Frequency Response Analyser

Technical Manual – Volume 1

MP MASTER



MA20022

SOLARTRON

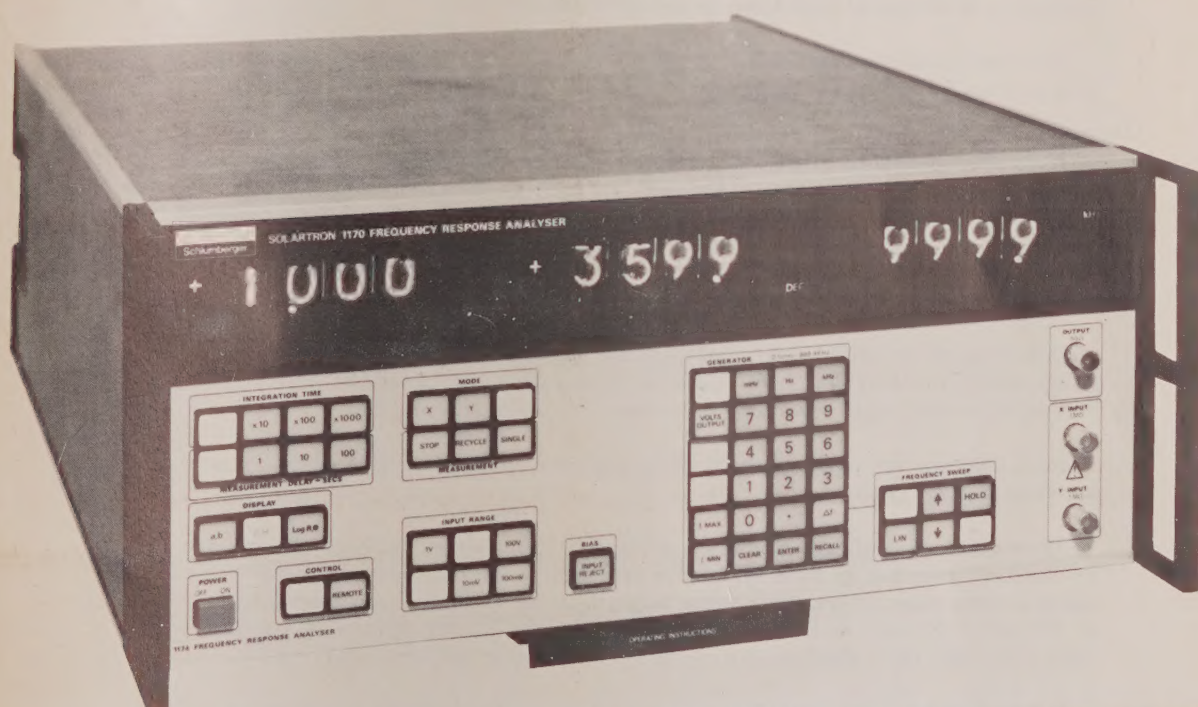
Schlumberger

1174

Frequency Response Analyser

Volume 1

OFFICIAL RECORDS STATION
FILE COPY
FACILITIES AUG 5 5 59 91



SANGAMO WESTON

Schlumberger**Solartron Instrumentation Group**

Sangamo Weston, Inc.

17972 Sky Park Circle, Suite F, Irvine, CA 92714

Tel: (714) 641-7137

Part No. 11740200

Issue 1 : March 1978

Schlumberger

THE SOLARTRON ELECTRONIC GROUP LIMITED
FARNBOROUGH HAMPSHIRE ENGLAND GU14 7PW
TEL: FARNBOROUGH 44433 (STD 0252)
CABLES: SOLARTRON FARNBOROUGH HANTS
TELEX: 858245 SOLARTRON FARNBOROUGH

TECHNICAL MANUAL

Arrangement of the manual

The manual is divided into two main sections. Volume (Section) 1 includes the functional description, circuit diagrams, and description of diagnostic equipment. Volume (Section) 2 includes a description of the instrument assembly, parts lists, pcb layouts and interconnection summaries.

A separate manual contains the equivalent information for the peripheral units which occupy positions 18 to 22 of the mainframe.

How to use this manual

The following notes are intended to help the user derive maximum benefit from using the manual.

This manual gives information for the 1174 Frequency Response Analyser only. As the 1174 requires virtually no routine servicing, this manual is primarily intended to assist the Service Technician in the task of fault diagnosis and rectification.

In common with the other models of the 1170 series, the 1170 mainframe is used, but the 1174 plug-in is unique to the 1174 instrument.

There are many signals within the instrument, and to avoid ambiguity these are numbered as well as named. Those used within the 1174 plug-in have numbers from 800 upwards. Printed opposite each circuit diagram is a table of signals used on that diagram giving the numbers of other circuit diagrams to which the signals are taken. At the back of Volume 2 is the Interconnection List which lists the signals in numerical order, gives their names and their interconnection by edge-connector and board (as against circuit diagram).

Certain signals are named in terms of frequency bands, but these frequencies are only approximate serving merely to clarify the signals' functions. An example is the signal 0.2–2MHz which, on the two top frequency ranges, can in fact lie between 180 kHz and 1997.8 kHz.

Block diagrams throughout the body of the descriptive parts of the text help to explain the significance of the signals.

The majority of circuit diagrams relate to circuitry on more than one board, grouping being made by function rather than by location. Circuits pertaining to one board only are mostly those of the digital section, where division by function largely becomes meaningless, and those of the 1174 plug-in. The circuit diagrams are listed on page 1.4.1 and on the following page is the Circuit Diagram Allocation Chart which gives the relationship between boards and circuit diagrams.

It should be noted that the 1174 plug-in boards are numbered separately from those of the mainframe; thus, for example, these are two distinct Boards 8, one in the mainframe and one in the plug-in. There are two mainframe Boards 5, being used for very similar functions, and no Board 6. No mainframe Board 9 exists, the appropriate slot being empty. Each of the plug-in types has unique boards. Note also that circuit differences exist between mainframe Boards 24 for use with the 1174 and 1172 or 1177 plug-ins.

The 1174 plug-in mother board is numbered 18 and a labelled copper artwork is included with the circuit diagrams to show at a glance the interconnections between the plug-in boards.

The plugged connections J and K between the mainframe and plug-in have their contacts listed in Volume 2 (see "Order of Pages" on page 2.3.4), and the contact positions of Socket J (SKJ) are drawn on the 1170 PCB No. 25 (mainframe mother board) layout diagram.

Contents	Page
Section 1 — Functional Description	
1.2 Rectification Techniques	1.2.1
Appendix A — Special test equipment	1.2.A1
Appendix B1 — Store state indicator	1.2.A3
1.3 Technical Description	1.3.1
Introduction to machine organisation	1.3.3
Introduction to the generator	1.3.9
The input system	1.3.15
Selector latching	1.3.20
Correlation in the 1174	1.3.31
Introduction to the arithmetic unit	1.3.37
Introduction to board 3 (mainframe)	1.3.47
Introduction to board 8 (mainframe)	1.3.49
Exponent counter	1.3.53
Decode logic	1.3.54
The arithmetic registers	1.3.57
Introduction to sequence logic	1.3.65
Introduction to control logic	1.3.70
1.4 Circuit Diagrams	
List of circuit diagrams	1.4.1
Circuit diagram allocation chart	1.4.2
Circuit diagrams 1–74	
The display unit (circuits 74 and 75)	
Appendix B2 — Store state indicator (circuit 76)	

Solartron pursue a policy of continuous development and product improvement. The specifications in this document thus may be changed without notice.

Section 1

Functional Description

INTRODUCTION

This section is divided into three sub-sections, namely:-

- 1.2 Rectification techniques
- 1.3 Technical description
- 1.4 Circuit diagrams



Digitized by the Internet Archive
in 2025

1.2 RECTIFICATION TECHNIQUES

Introduction

The purpose of this Servicing Manual is to assist the reader in the task of fault rectification, and like any other electronic equipment, fault rectification on the 1174 is carried out in chronological steps which may be summarised as follows:-

- 1) Definition:- The fault is defined in terms of the published specification for the instrument.
- 2) Diagnosis:- The faulty or maladjusted components or assemblies are isolated.
- 3) Replacement:- Faulty components or assemblies are removed and replaced with serviceable items.
- 4) Adjustment:- Any variable components affected by the fault are adjusted to the limits defined in the calibration procedures.
- 5) Performance check:- To ensure that the whole instrument is performing within the published specification.

A competent service engineer will find it possible to rectify many faults using standard test equipment and the information contained in this manual. More complex faults, including any which require adjustment after component replacement, will require the use of the special test equipment. A list of this equipment is given in appendix A to this sub-section.

It should be noted that calibration instructions are included as part of the special test equipment and are not given in this manual.

ACCESS

Most parts of the instrument are accessible with ease. Figs. 2.2.1. to 2.2.5. should be consulted to determine the location and method of assembly of the various parts. Extension boards and leads are available (see special test gear list) to enable any board to be worked on in situ.

CAUTION

An extension lead, Type No. TG 1212R, is available allowing operation of the 1174 out of the mainframe. When fitting this lead observe the following procedures:-

1. Switch off power.
2. Fit the cable, making sure the plugs and sockets are correctly orientated and secure before switching on the power.

Severe damage may result if the cable is plugged in with power on and incorrect pin mating.

FRONT PANEL TOUCH KEYS

Care must be taken when replacing lamps in these keys. A metal deposition on the glass cover forms the touch plate. This is connected to the circuit by means of the spring clips which also form the cover securing clip. Care must, therefore, be taken that the springs are not distorted and that good contact is made with the plate upon replacement. The contact clip on the touch button cover must be flush with the inner side.

DISPLAY UNIT

If the display unit is to be serviced it is necessary to remove the whole unit and support it clear of the case. Great care must be taken during this operation to ensure that an insulating sheet is placed under the display unit. 200V is generated within the display unit. This voltage can destroy parts of the instrument or cause injury to the user, if great care is not taken.

FAULT DIAGNOSIS

For the purposes of fault diagnosis and rectification the instrument may be regarded as consisting of several major functional areas.

The following block diagram defines these major areas.

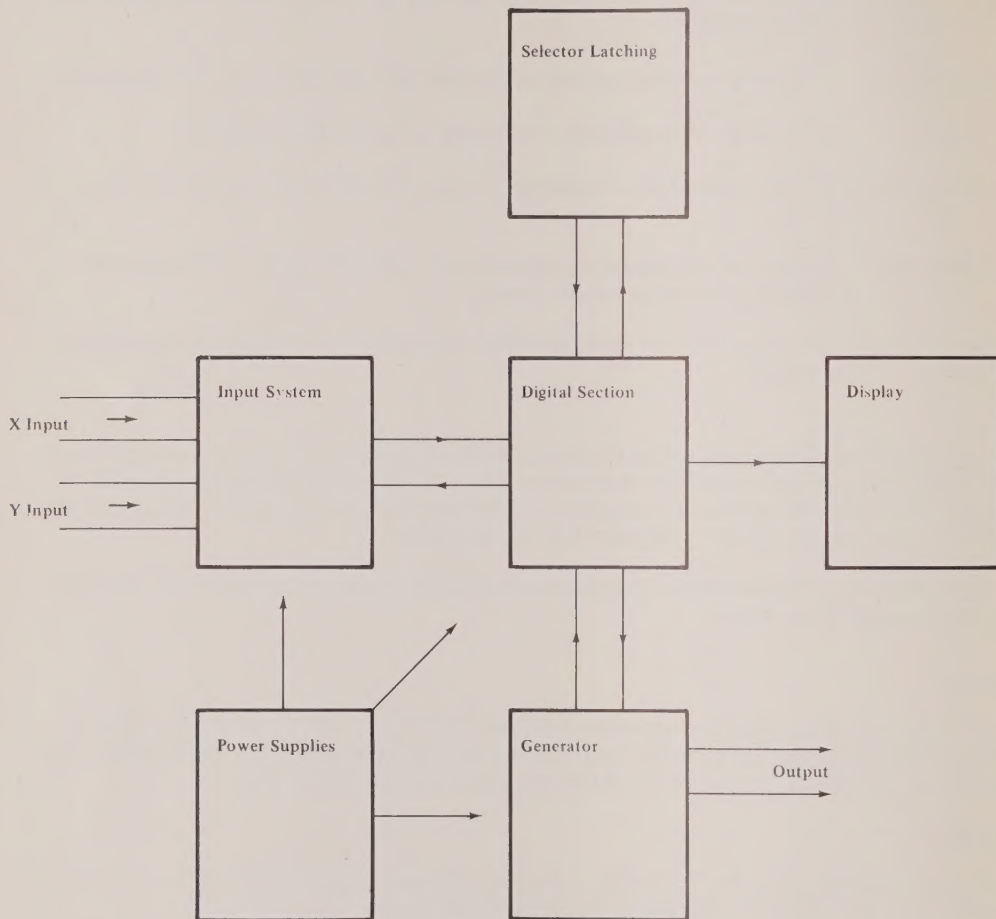


Fig. 1.2.1

Reference should be made to the 1174 Circuit Diagram Allocation Chart, which appears in both Sections 1 and 2, where all circuit diagrams and printed circuit boards for each of the areas are listed.

The type of fault diagnosis that may be attempted depends, to a large extent, upon in which of the areas the fault falls.

An item of special test equipment is available which assists in fault location; namely the Store State Indicator Type TG1212A.2, available from your Schlumberger agent. See Appendix B.

When the faulty area has been located, rectification action will vary between the areas. A description of the recommended treatment for each area is given in the following paragraphs.

POWER SUPPLIES

Fault finding may be carried out using traditional methods in this area. After rectification a certain amount of re-calibration may be required.

INPUT SYSTEM

Servicing in this area requires use of the techniques used on most high accuracy measuring instruments. Signals may be followed using standard test equipment.

The control of the circuits in this area originate in the digital section. Many of the signals are coupled with optical couplers.

This area contains many variable components. Therefore in many cases re-calibration will be required after fault rectification.

DISPLAY

This area consists of a 200V generator, together with several neon indicating devices and associated decoding circuits. Servicing of this area is straight-forward but the decoding circuit will require careful study when diagnosing the more obscure faults.

No calibration of this area is necessary.

SELECTOR LATCHING

This area consists of an unconventional loop circuit best explained by the following diagram.

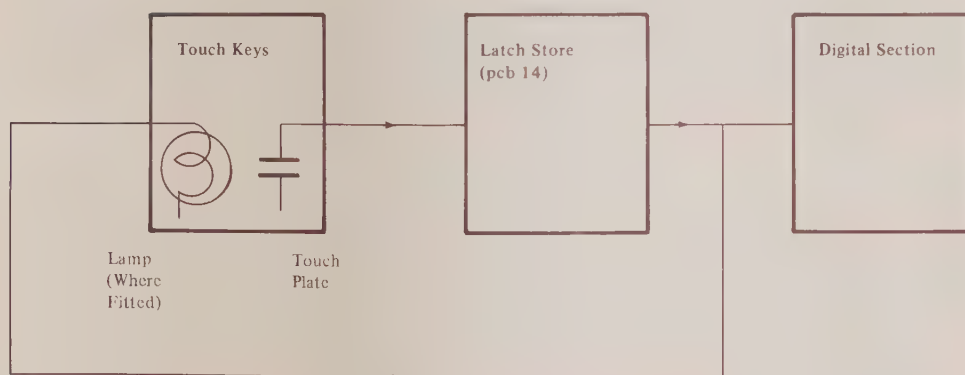


Fig. 1.2.2

When a touch button is touched, the appropriate latch store location is activated. The digital section uses this latch store information to perform the necessary actions; it is also passed back to the touch button, causing the lamp to light.

The data from the front panel are serialised before being passed to the latch store for decoding. The feed-back data is also in serial/parallel form.

Although fault-finding is possible, using standard test equipment, familiarity must be gained with the timing sequences used, before the data can be interpreted intelligently.

The most useful item of test equipment for use in fault finding is the Store State Indicator, and its use is strongly recommended. With this instrument one can examine the contents of any latch store location, or write-in a new selection without using the front panel. Intelligent use of the SSI will usually quickly establish the cause of a fault.

DIGITAL SECTION

This area is an arithmetic processor, digital store and digital control circuit. It uses techniques similar to those used in digital computers and the service technician should therefore be familiar with these techniques.

Attempting to follow signals through the circuits of this area will often prove abortive, and although simple faults may be diagnosed using standard test equipment, it is recommended that Complete pcb replacement is used to rectify the more complex faults.

To carry out an efficient repair service on this area it is therefore desirable to carry a spare set of serviceable mainframe pcb's No. 2, 3, 4, 5, 7, 8, 10, 11, 12, 13, 15, 16 and 17. A Store State Indicator TG1212A2 as used in the Selector Latching area is also recommended.

Determination of the faulty board or component within this area will often require a combination of:-

- 1) An examination of the contents of the appropriate MOS store locations by means of the SSI.
- 2) A knowledge of the operation of each of the pcb's.
- 3) An intelligent interpretation of the indications of unserviceability, as shown by the effects on other areas of the instrument.
- 4) In certain cases, a degree of trial-and-error by substituting pcb's and observing the effect. This must, of course, be used with discretion to avoid causing further faults.
- 5) If a second 1174 FRA of known serviceability is available, a rapid method of fault location by means of pcb exchange between the two instruments may be used. Care must of course be exercised to prevent damaging the serviceable instrument. For this reason this method should not be used if a fault is suspected to be in the power supplies or associated circuitry.

APPENDIX A – SPECIAL TEST EQUIPMENT

The service kit (part number 11706000) for the 1170 series of Frequency Response Analysers comprises all the equipment described in this appendix, having a TG1212 number or an 1174 number. A kit (number 11746000) is available for converting a TG1212 kit (no longer available separately) to the complete 11706000 kit.

TYPE No.	ITEM
TG 1212A.2	Store State Indicator
* TG 1212 BB	Square Wave Calibrator Unit
* TG 1212 CC/1	Straight through
* TG 1212 CC/2	20 dB Attenuator
* TG 1212 CC/3	40 dB Attenuator
* TG 1212 CC/4	60 dB Attenuator
* TG 1212 CC/5	1184 90° Phase Unit
* TG 1212 CC/6	Fundamental Rejection Filter
* TG 1212 CC/7	Harmonic Rejection Filter
TG 1212 D/18	P. Supply Lamp Monitor Board
TG 1212 D/22	Carries P.S. Lamp Monitor and Loading board
TG 1212 D/23	Input system Lamp Monitor and Loading board
TG 1212 IA	1170 Extension board
TG 1212 IB/1	1172 Extension board (24 way)
* TG 1212 IB/2	1172 Extension board for Bd 11 (with additional inverter protection Resistors – for fault finding).
* TG 1212 IB/3	D-A Programme board – simplified
* TG 1212 C	1172 Extension board – 16 way
TG 1212 L	Display Test Set
TG 1212 P	P. Supply Pulse Driver (position PCB 26)
TG 1212 R	1170 – 1172 Extension Lead
* TG 1212 T	Relay timing unit
TG 1212 X/3	5 volt loading board – 4 amps
TG 1212 X/9	5 volt loading board – 4 amps
TG 1212 X/13	5 volt loading board – 4 amps
TG 1212 X/16	5 volt loading board – 4 amps
TG 1212 X/14	5 volt loading board – 8 amps
TG 1212 X/19	18 volt loading board – 3 amps
TG 1212 X/20	18 volt loading board – 8 amps
	Production Test Specification
	(Full calibration instructions and testing)

* Note: Not useful for 1174 but supplied in kit.

For the 1174 Update Service Kit, see overleaf.

The 1174 Update Service Kit (part number 11746000) comprises the following:—

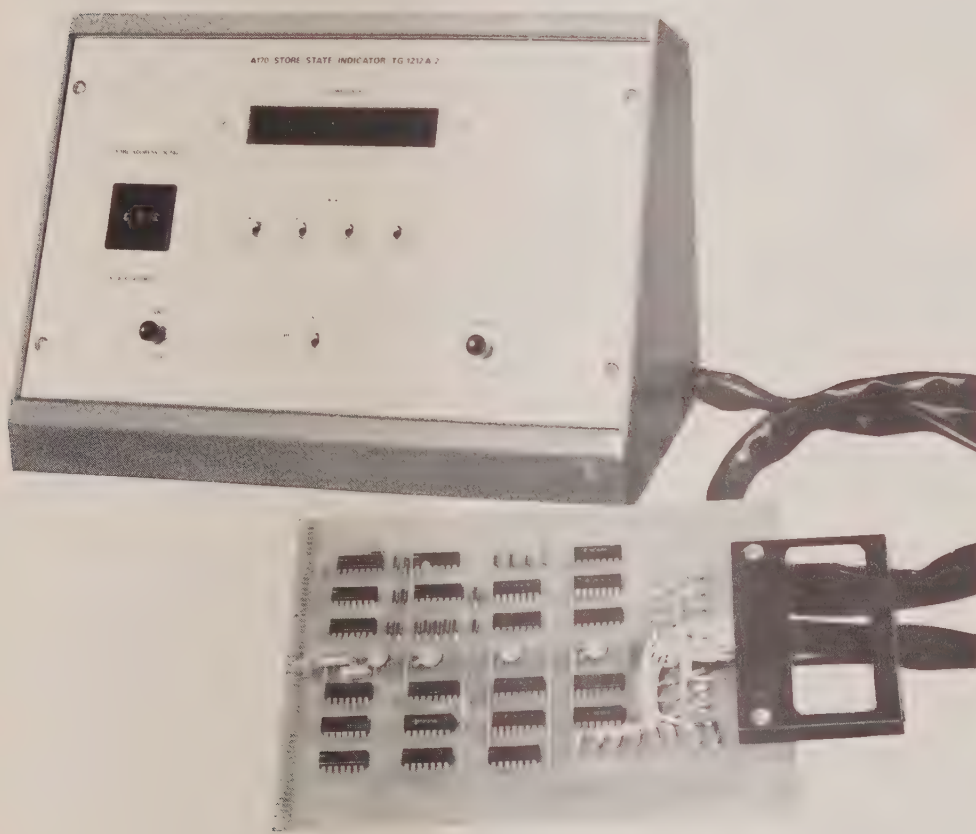
TYPE No.	ITEM
11746002	Sine to square converter
11746003	1kHz notch filter
11746004	Thermocouple frequency response tester
11746005	Low-pass filter
11746006	Diode clipper unit
11746007	Coax lead 1m BNC-BNC
11746008	Coax lead 1m BNC-4mm
11746009	20/40 dB resistive attenuator
11746010	40 dB capacitive attenuator
11746014	Pcb 14 extension lead
11746015	Dc bias box
11746016	High-frequency high-voltage resonator
11746017	24 way extension board
351001450	50 ohm BNC termination
354000410	50 ohm BNC T junction
11746030	Transit case
11740139	Test specification
11740147	Test procedure

Appendix B1 – STORE STATE INDICATOR

Introduction

This instrument is an item of test equipment used for fault diagnosis and calibration of the 1170 series of Frequency Response Analysers.

The 1170 contains two major storage systems, called respectively the MOS store and the Latch store. The Store State Indicator (SSI) enables the contents of these stores to be examined and data to be written directly into them.



1170 Store State Indicator (TG 1212 A2)

SSI OPERATING INSTRUCTIONS

Principle

The eight LED numerical indicators continuously read the data held in selected locations of the MOS or Latch stores. If “MOS” is selected the display will show the contents of the eight locations of the group selected by the first and third thumbwheel selector switches. If “Latch” is selected the data held in two locations will be displayed. In this case the data will be displayed four times in alternate windows. A complete list of selections is given later, in tabular form.

The second thumbwheel switch and the four data switches are used to write-in new data as an alternative to the use of the Frequency Response Analyser (FRA) front panel.

Applications

The SSI has two main applications; fault location and calibration.

For fault location the SSI is used to read the contents of the stores directly so by-passing the FRA display or touch-key indicators. Data may also be directly inserted into the stores from the SSI, so by-passing the touch-keys and, in certain cases, parts of the arithmetic and measuring systems.

It is impossible to list all the instances in which these facilities may be used but after some practice the operator will soon realise its full usefulness.

For calibration purposes the SSI has two facilities which make it almost indispensable. Firstly it may be positioned so that the duplicated display may be viewed from the rear of the FRA, where the adjustments are made. Secondly, the SSI displays two more significant digits than the FRA display. The FRA in its arithmetic processor computes to two decades more than are displayed or specified. The viewing of these two digits by the SSI enables the operator to make setting-up adjustments to a higher degree of accuracy than by the use of the FRA display alone.

Before using the SSI it is necessary to acquire a working knowledge of the stores.

The MOS Store

The store is IC5 on pcb No. 12 of the 1170. The circuit is found on Diagram No. 66. It contains a maximum of 256 four bit words.

In this store are contained all the results of the various computations made during the correlating process, together with the parameters of voltage and frequency commanded from the front panel.

The SSI allows the contents of eight of the locations to be read at one time or data to be written into one of them. The location to be written into or the group to be read is selected by the Selector switches which form an assembly of three octal coded thumbwheel switches, allowing selection of 0 to 377₈. (0 to 255 in decimal notation). Conversion from octal to decimal radices is explained later.

A table showing the contents of the various locations is given later, together with the SSI operating procedures.

The Latch Store

This store occupies most of pcb No. 14 and part of pcb No. 16 of the 1170. The storage elements are D type flip-flops and are found on Diagrams 32 to 36.

The store contains data which defines all the selections made on the front panel touch buttons. (The required measurement parameters are held in the MOS store).

The SSI allows the examination of any of these locations and the direct writing-in of data.

A table of the switch selections necessary, and the contents of the store is given later, together with the operating procedures for the SSI.

Timing

Access is made to the various locations of both stores by means of strobe pulses originating in the SSI.

Each of the 256 locations of the MOS store is connected to the 4 input and 4 output busses, in turn, by a 500kHz clock. A synchronising pulse is used to begin each 256 pulse sequence. The timing of the strobe pulse is decided by the settings of the selector switches. Thus the selection indicates the time slot allocated to each of the locations. This information is of use if it is desired to view the bus data by means of an oscilloscope.

The selection is in octal code. It is therefore necessary to convert to decimal and count from the synchronising pulse to identify a location. For instance, Table 1, shows that the 3rd digit of θ (Y) in radians is found on selection 264 (= 180 dec). This location will therefore be connected to the busses 180 pulses at 500kHz after the synchronising pulse.

The same sequence of 256 pulses that are used to clock the MOS store are used for the Latch store. But in this case only the first 16 pulses are required.

The timing sequence, which, it will be noted, is the reverse of the address switch selection is as follows:-

1st pulse. No. 7 of second column (Harmonic selector) of Table 2.



8th pulse. No. 0 of second column (Sweep mode)



9th pulse. No. 7 of first column (Sweep command)



16th pulse. No. 0 of first column (Integration time)

Operating Instructions

Installation

It is recommended that the SSI interface board is plugged into position 18 of the 1170 although position 20 may be used if 18 is occupied. No other connections to the SSI are required. The 1170 power switch should be off when the SSI is inserted.

Operating Procedures

MAINS SET - Operation of this switch sets all stores to the state at power switch-on. It must not therefore be operated unless this state is intended.

MOS/LATCH selector - Operating procedures after this selection is made differ slightly. They are therefore treated under separate headings.

MOS

Refer to Table 1. To read the data in a group of store locations select on the first and third bank of the selector switch the required numbers. The data contained in the location for each of the eight digits will be shown in the appropriate window.

5th and 6th Significant Digits

The display of each measurement by the 1174 is to four significant digits, but it will be noted that the SSI displays the same data to six significant digits, the last two being used for correlation processes but not displayed.

Write-in

To write-in data the first and third selector switches must be set to the appropriate group, and the centre switch set to the digit into which new data is to be written.

The data is then set on the four data switches.

Switch Up = 1

Switch DOWN = 0

e.g. To write-in value 6:- SW8 ↓, SW4 ↑, SW2 ↑ and SW1 ↓.

Next press and release the *write* button and observe that the data shown in the selected digit window has changed to the new value.

Unused Addresses

The addresses marked N.U. may contain data, but interpretation is impractical. Address 0n0 may contain data if an 1185 Synchroniser is fitted. The other addresses contain temporary data used in the computation processes.

Latch

As the latch store occupies only 16 locations, the first of the Store Address selector switches is not used and can remain on any selection.

To read the contents of a location, only the third selector switch need be set, when the contents of two locations will be observed simultaneously. Care must be taken when reading, as each item of data is repeated four times in alternate windows. *Table 2* lists the locations and an interpretation of the data they may contain.

Write-in

As well as the third Selector switch, to write-in, the second (Decade Address) must also be set to either 1 or 0, depending on in which column the required location appears in table 2. Also "Remote" must be selected on the FRA front panel.

The data to be written in is then set in BCD on the four data switches,

Switch UP = 1

Switch DOWN = 0

e.g. To write-in the selection -ve BIAS, the data value 6 must be inserted into the Keyboard group location, which (from Table 2) requires the selection of X11 on the thumbwheel switches. The data (6) is then selected:- SW8 ↓, SW4 ↑, SW2 ↑, SW1 ↓.

The "write" button is then pressed and the display observed to check that the data has changed in the four appropriate windows. i.e. windows 0, 2, 4 and 6 will show 6 in the case used as the example.

Input Range

Selections 5 and 6 require some care when reading or writing. Location 5,0 contains data on the input range in use by the 1170. The data can only be input to this location via selection 6,0. Location 6,0 contains data showing whether a fixed range or auto is selected. Therefore if any fixed range is selected, this store (6,0) will only show data 0 but location 5,0 will show the actual range. If auto is commanded location 5,0 will show the range in use.

Octal to Decimal Conversion

Take octal number 5 2 3 4

$$\begin{array}{rcl}
 & & = 4 \times 8^0 = 4 \times 1 = & 4 \\
 & & = 3 \times 8^1 = 3 \times 8 = & 24 \\
 & & = 2 \times 8^2 = 2 \times 64 = & 128 \\
 & & = 5 \times 8^3 = 5 \times 512 = & 2560 \\
 \hline
 & & & 2716 \\
 \hline
 \therefore 5234_8 = 2716_{10}
 \end{array}$$

Octal weightings

$8^0 =$	1
$8^1 =$	8
$8^2 =$	64
$8^3 =$	512
$8^4 =$	4096
$8^5 =$	32768
etc.	

Octal to Binary

$1_8 =$	001
$2_8 =$	010
↓	
$7_8 =$	111
$10_8 =$	001 000
↓	
$77_8 =$	111 111
etc.	

MOS STORE

Notes to Address Chart

- To read. Select 1st and 3rd Switch selection [Store Address (Octal)]. The eight windows show the data held in the selected location.
- To write. Select 1st and 3rd Switch selection. Select digit to be written into on 2nd switch (Decade address). Select data value (up = 1 down = 0). Press "write" switch.

- On table 1:-

1 = Most significant digit

2 = 2nd

3 = 3rd

4 = 4th (Least significant digit of display)

5 = 5th

6 = Least significant digit in store

Ex = Exponent. The value is given in "notes"

O/L = Overload

- Shaded digits. Any data shown in these spaces should be ignored.

- Notes on individual addresses.

1n0 to 3n2 These are measured values held in the stores (except those not used, n.u.)

0n3 Add Bias. As commanded from front panel. *

1n3 Log f. The logarithm of the data held in location 2n7.

2n3 $V_{OUT} (DISP)$ The value (numbers only) commanded from front panel (See 0n7).

3n3 Bias (Rej) As measured when "input reject" is commanded. This value is not displayed on 1170.

1n4 to 3n5 Measured values.

0n6 to 3n6 Frequencies as commanded from front panel.

0n7 $V_{OUT}(OP)$ The generator output voltage.

2n7 $f_{OUT}(OP)$ The generator output frequency.

3n7 Δf_{LOG} . Number of measurements per decade as commanded from front panel.

377 is Mains set command when written-in.

CONTENTS	SWITCH SELECTION	0	1	2	3	4	5	6	7	NOTES
N.U.	0	0								1185 Period Data
R (X)	1	0	1	2	3	4	5	6	7	Ex 2 xxxxxx mV 4 xxxxxx V etc
R (Y)	2	0								
R (Y/X)	3	0								
N.U.	0	1								
a (X)	1	1	1	2	3	4	5	6	7	Ex as R
a (Y)	2	1								
a (Y/X)	3	1								
N.U.	0	2								
Log R (X)	1	2	1	2	3	4	5	6	7	
Log R (Y)	2	2								
Log R (Y/X)	3	2								
ADD BIAS	0	3	1	2	3	4	5	6	7	
Log f	1	3	Ex	Ex	1	2	3	4	5	Ex 04 1Hz to 10Hz 07 1kHz to 10kHz etc
$V_{OUT} (DISP)$	2	3	1	2	3	4	5	6	7	
BIAS (REJ)	3	3	1	2	3	4	5	6	7	Ex as R POL. 1 = Rej. +ve 0 = Rej. -ve
N.U.	0	4								
$\theta (X)$	1	4	1	2	3	4	5	6	7	
$\theta (Y)$	2	4								
$\theta (Y/X)$	3	4								
N.U.	0	5								
jb (X)	1	5	1	2	3	4	5	6	7	Ex as R
jb (Y)	2	5								
jb (Y/X)	3	5								
fMAX	0	6	1	2	3	4	5	6	7	Ex 1 xxxmHz 4 xxxHz 7 xxxkHz etc
fMIN	1	6	1	2	3	4	5	6	7	
f (DISP)	2	6	1	2	3	4	5	6	7	
Δf_{LIN}	3	6	1	2	3	4	5	6	7	Ex
$V_{OUT} (OP)$	0	7		1	2	3	4	5	6	Ex 1 = .01V Range 2 = 0.1V 3 = 1V
N.U.	1	7								
f (OP)	2	7	1	2	3	4	5	6	7	Ex as fMAX
Δf_{LOG}	3	7	1	2	3	4	5	6	7	M SET Write M.SET to clear all stores.

TABLE 1. MOS STORE ADDRESS CHART
(Before use see notes)

*Not used in 1174

3rd switch selection	COLUMN 1		COLUMN 2	
	To write, select 0 on Decade Address, with third Store Address switch as shown on left. To read, select third Store Address as shown and read windows:-		To write, select 1 on Decade Address, with third Store Address switch as shown on left. To read, select third Store Address as shown and read windows:-	
0		Integration Time		Sweep Mode
	0	MIN	0	LIN
	1	x 10	4	LOG
	2	x 100		
	3	x 1000		
1		Measurement Delay		Keyboard
	0	MIN	0	t_{MIN}
	1	1	1	t_{MAX}
	2	10	2	f_{REQ}
	3	100	3	t_{INCR}
			4	O/P V
			5	+ve BIAS *
			6	-ve BIAS *
2		Display Co-ordinates		Frequency Range
	0	Polar ($R\theta$)	0	mHz
	1	Cartes ($A + jB$)	1	Hz
	2	LOG $R\theta$	2	kHz
3		Measure		Generator Mode *
	0	X - Y (not used)	0	Ramp
	1	X	1	Sine
	2	Y	2	Square
	3	Y/X		
4		Measure Sequence		Carrier Modes *
	0	Stop	0	Normal
	1	Re-cycle	1	Mod O/P
	2	Single	2	Demod I/P
	3	Stop (end of cycle)	3	Mod O/P Demod I/P
5		Input Range		Bias Mode
	2	10mV	0	Normal
	3	100mV	1	Add bias *
	4	1V	2	Reject bias
	5	10V	3	Add & Reject bias *
	6	100V		
		Read Only		
6		Input Range		Local/Remote
	0	Fixed	0	Local (If Local is
	2	10mV	1	Remote written-in,
	3	100mV	2	no further data can be
	4	1V	3	written until Remote
	5	10V		is commanded on front
	6	100V		panel).
	8	AUTO		
		Write Only		
7		Sweep Command		Harmonic Selector
	0	OFF		(Used with extension
	1	HOLD		units)
	2	UP		
	3	DOWN		

TABLE 2. LATCH STORE ADDRESS CHART

*Not applicable in 1174

1.3 TECHNICAL DESCRIPTION

This section, when read in conjunction with section 1.4, provides a description of the instrument in both a theoretical and functional form.

An introductory section describing the various processes used in the 1170 system is followed by a functional description of the instrument, using block diagrams with direct reference to the circuit diagrams. This serves to describe the analogue parts of the instrument, the digital sections being described in a mainly theoretical fashion at the end of this sub-section.

INTRODUCTION TO MACHINE ORGANISATION

The 1174 is divided into two parts - the "Generator" section and the "Analyser" (correlator) section.

The Generator section produces an electrical sine wave output signal. The amplitude and frequency of this signal are controlled from the keyboard.

The Analyser accepts an electrical input signal, and, when commanded from the keyboard, makes a measurement on this signal and displays the results.

Measurements may be made on either of two input channels (channel X or Y), and the most recently measured results on either channel (X or Y), or the ratio between them (i.e. "point to point" result, Y/X) may be displayed. The results may be displayed in any of three co-ordinate systems (A and jB , R and θ , or $\log R$ and θ).

The instrument contains a data store (MOS STORE), in which are stored all the results, as well as the generator operating parameters, and the frequency sweep parameters. It also contains an "arithmetic unit", which is used to calculate the results, and a "control logic" section, which controls the overall sequence of operations performed by the machine.

The generator parameters and frequency sweep parameters may be altered from the keyboard when the instrument is not measuring. Some action by the control logic and arithmetic unit is necessary when changing the generator parameters - the frequency sweep parameters may be changed directly via the keyboard. Any one of these parameters may be displayed in the "Keyboard Display", by touching the appropriate key.

The "Results Display" can display any one set of results from the store in accordance with the setting of the A, B; R, θ ; $\log R$, θ and X; Y; Y/X keys.

MEASUREMENT SEQUENCES

The simplest measurement which the machine can make is with the following front panel touch key settings:

Sweep OFF
SINGLE Measurement
Channel X
Reject Bias OFF
Fixed input voltage range

To make a measurement under these conditions, the input is first analysed by the "correlation" process (see CORRELATION IN THE 1174). This gives an intermediate result, which, after division by "integration time", T (by the arithmetic unit), provides results in A, jB form which are placed in the MOS store. Further calculation by the arithmetic unit gives the single channel results in the other co-ordinate systems, which are also stored. The "point to point" results are then calculated and stored, using the previously measured results for channel Y from the store.

The other functions which can be provided by the instrument, when requested from the touch keys, are accomplished as follows:

1. **Autorange** Measurement starts on the 10mV range. If the instrument overloads, the measurement is terminated immediately, the input range is increased by a factor of 10, and a new measurement commenced. This is repeated, if necessary, until the 100V range is reached.
2. **Reject Bias.** A measurement is made in the "Measure bias" mode. The single channel calculation proceeds to the point where the in-phase component (real part) is known. A voltage of this magnitude is then generated internally and applied as a "backing-off" voltage to oppose the bias, and a new measurement taken.
3. **Point to point.** A set of relays ("input relays") is provided so that the input of the analyser can be connected either to the channel "X" connector or to the channel "Y" connector. A channel "X" measurement is taken and the single channel results calculated and stored. The input relays are then changed to channel "Y", and another measurement taken, and single channel and point to point results calculated and stored.
4. **Frequency sweep.** Before the measurement, a new frequency is calculated by the arithmetic unit, using the parameters which have been entered into the store from the keyboard (f_{MIN} , f_{MAX} , Δf_{LOG} , Δf_{LIN}). The generator frequency is changed to this new frequency. A delay depending on the setting on the "measure delay" touch keys is then allowed to elapse before commencing the measurement. This allows any transient in the "system on test", due to the change in frequency, to die away.
5. **Recycle** A continuous series of measurements is initiated. Between each measurement, a delay is allowed to elapse depending on the setting of the "measure delay" touch keys.

FUNCTIONAL DESCRIPTION

The functional description is based upon the following block diagram, which forms the highest level of description.

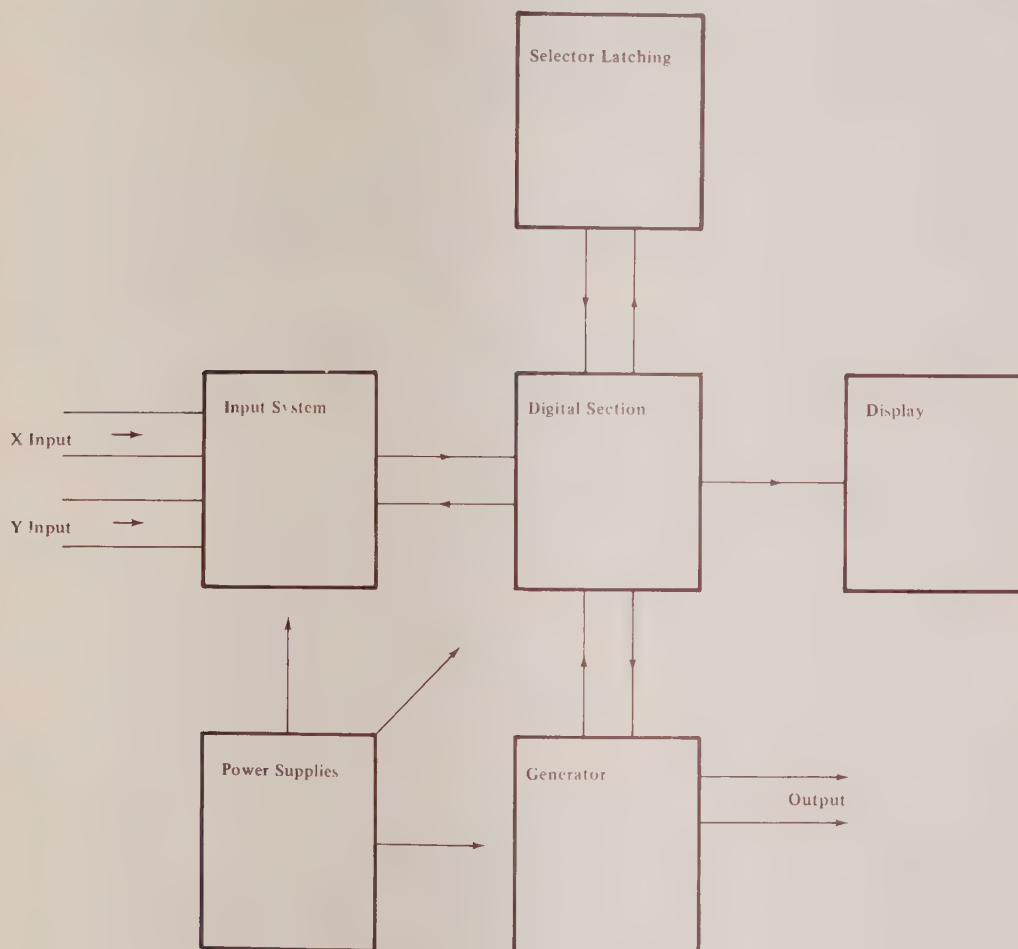


Fig. 1.3.1

The second level **takes** each of the areas shown in the first level diagram and breaks it down into a series of block diagrams, which make direct reference to the circuits and physical interconnections.

The third level of description is the circuit diagrams proper found in section 1.4. Where necessary a description of the circuit diagram, and a list of its connections with others, is given on each opposite page to the circuit diagram.

Due to its complexity and the nature of its signals it is not possible to cover the digital section in the same way as the others. For this reason a theoretical description of the digital section is given after the functional description. The description is mathematically orientated and uses terms and descriptions used in the design of digital computers. This description is of limited use in a servicing environment but should be studied if a full understanding of the working of the 1174 is required.

The display system is shown as an adjunct to one of the digital section block diagrams.

BLOCK DIAGRAMS

Except for the two diagrams showing the digital section, the block diagrams are arranged in a common format. Each block represents a circuit diagram, the number of which heads the text within the block, the name of the diagram and the numbers of pcs illustrated in the diagram then follows. Except where indicated by arrows, the main functional paths flow left to right across the diagram. Annotated numbers on the connections indicate the signal in the main interconnection list (Section 2.4.).

Control functions enter the blocks from top, bottom, left or right. The boxed annotations indicate:-

1. The circuit number to which they are connected.
2. The pcb number to which they are connected.
3. The signal name.
4. The interconnection number (in brackets) relating to the list in section 2.4.

Instead of circuit numbers some connections show the following:-

1. DIST. Indicates that it is connected to several circuits.
2. PERIPH. It is connected to one of the peripheral units in positions 18 to 22.
3. DISPLAY. Connected to the display.

POWER SUPPLIES



All supplies are derived from a +30V unregulated rail in Circuit No. 42. Voltage regulators in Circuit No. 43 are controlled by the sensing amplifiers in circuit No. 45.

The sensing amplifiers in circuit No. 45 are switched at 25kHz, by a clock which is derived from the floating supplies, circuit No. 44, which is in turn driven by a 100kHz clock from circuit No. 2 (in the mainframe).

Protection circuits are shown in circuit No. 43.

The mains set signal although not part of the power supply circuit is included as it is distributed via pcb No. 26, the power supply regulator board.

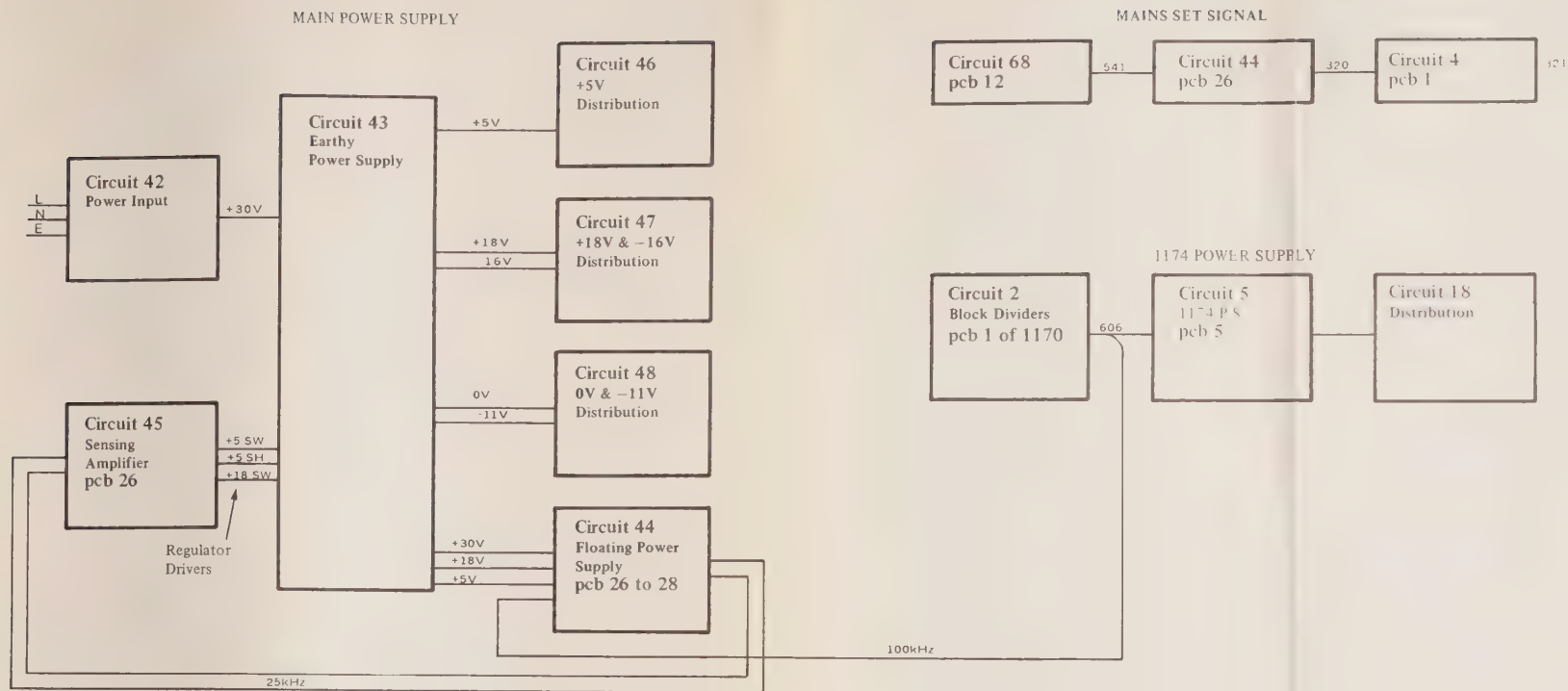


Fig. 1.3.2
POWER SUPPLIES

INTRODUCTION TO THE GENERATOR

This section includes circuitry responsible for a variety of functions. It provides reference frequencies, generates and controls signals at the output frequency of the instrument (achieving this in various ways in different frequency bands), and provides signals needed by the input and correlation circuitry. Understanding of the following description will be aided by referring to Fig. 1.3.4.

THE MASTER OSCILLATOR

A crystal controlled oscillator running at 20MHz acts as the reference for all important frequencies within the instrument. Digital dividers produce secondary frequencies. The 20.2-22MHz VCO and both the 20.002 and 20.020 MHz oscillators (part of the input system) are phase-locked to the master oscillator.

THE SYNTHESIZER

The heart of the synthesizer is the 20.2-22MHz VCO. On frequency ranges below 10kHz, the instrument's output signal is generated digitally using the signal GENERATOR CLOCK, which runs at $2000f$ (where f is the output frequency) for f less than 1kHz, and $200f$ for f between 1 and 10kHz. The VCO output is mixed with 20MHz, the product (called SYNTHESIZER OUTPUT) having a frequency between 0.2 and 2MHz. After frequency division by the appropriate number of decades the signal GENERATOR CLOCK results.

For frequencies above 10 kHz the output signal is generated, solely using analog techniques, from the V.C.O. output.

On frequency ranges below 10kHz, the CORRELATOR CLOCK (which drives the measurement process) is derived from the GENERATOR CLOCK. For the top two frequency ranges the correlation process does not work at the signal frequency and instead runs at a fixed frequency of 1kHz, and its clock is derived within the mainframe from a constant 2MHz.

The 20.2-22MHz V.C.O. output is also used within the input circuitry on the two top frequency ranges, in the generation of the HET signal. This signal is always 1kHz lower in frequency than the measurement frequency, and by heterodyning with the input signal translates its frequency to 1kHz for the correlation process.

The V.C.O. frequency is determined as follows. By mixing with 10MHz, its frequency is translated to 10.2-12MHz nominal. Programmed instrument operating frequencies always consist of four digits and frequency decade information. Let these four digits be represented by the number N , which will be between 1000 and 9999 by definition. Circuitry known as the Programmable Divider within the mainframe is arranged to divide the 10.2-12MHz signal in frequency by $(2N + 100\,000)$. The resulting frequency is phase-locked to a reference 100Hz by altering the 20.2-22MHz V.C.O. control voltage. The V.C.O. frequency under phase lock will thus be $20\text{MHz} + 200N\text{ Hz}$, as required.

SYNTHESISER CONTROL

The 20.2-22MHz VCO is controlled by a phase locked loop consisting of circuitry on diagrams 12, 13, 3, and 4.

The required synthesiser output frequency is called from the digital section into Circuit No. 3 by the T10 and T9 control lines (543 and 542). When the required synthesiser output frequency is correct the loop is phase-locked and the output of Circuit No. 3 is at 100Hz.

If the synthesiser output frequency is not correct the comparison made between T9, T10 control lines and the VCO output (6.19, 620 into circuit No. 3) will not produce 100Hz. The effect is to produce an increasing or decreasing ramp voltage which is used in circuit 13 to adjust the V.C.O. and so bring the loop into phase lock.

An example of the waveforms which produce the frequency adjustment is shown in Fig. 1.3.3.

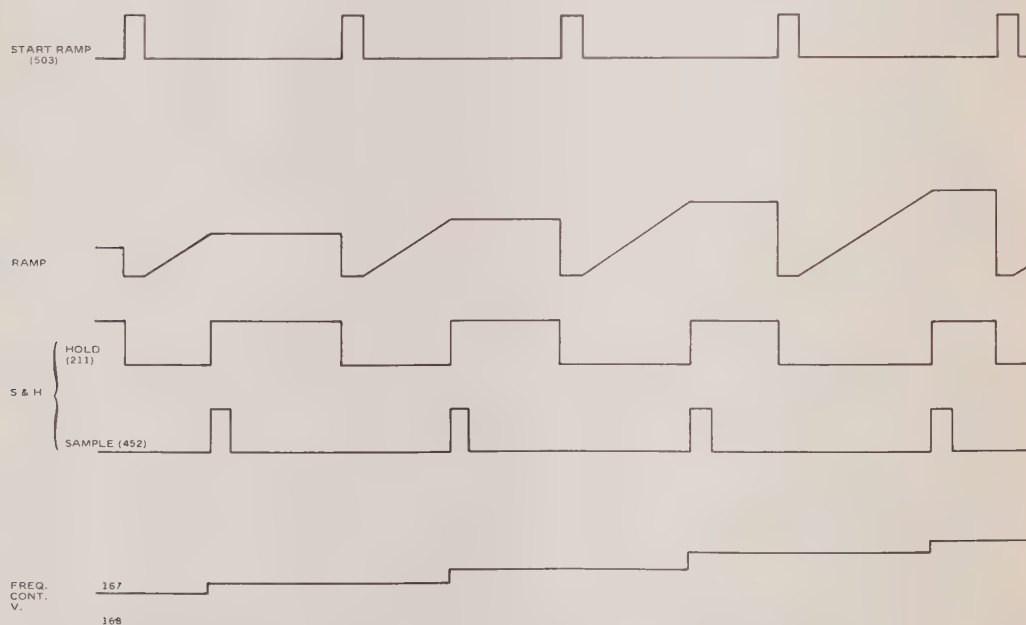


Fig. 1.3.3

In this example the frequency is low, causing the output prf of circuit 3, the sample and hold, to be below 100Hz. The start ramp signal from circuit No. 2, is fixed at 100Hz. The effect is, as shown, a low voltage to the VCO causing its output frequency to increase.

The increasing control voltage causes the synthesiser output frequency to increase until the output of Circuit No. 3, the sample and hold signals, is at 100Hz and the loop is phase-locked.

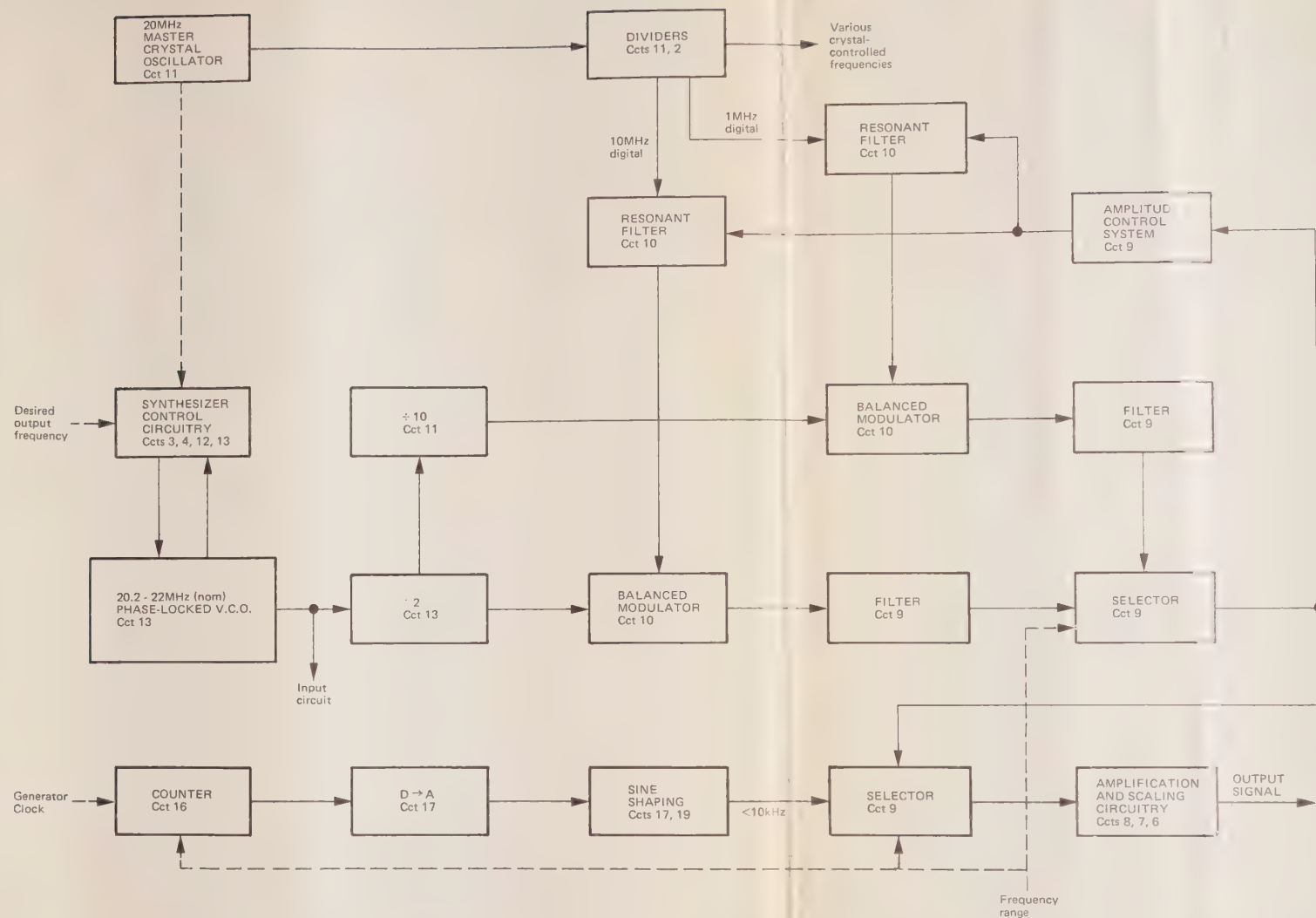


Fig. 1.3.4 1174 GENERATOR

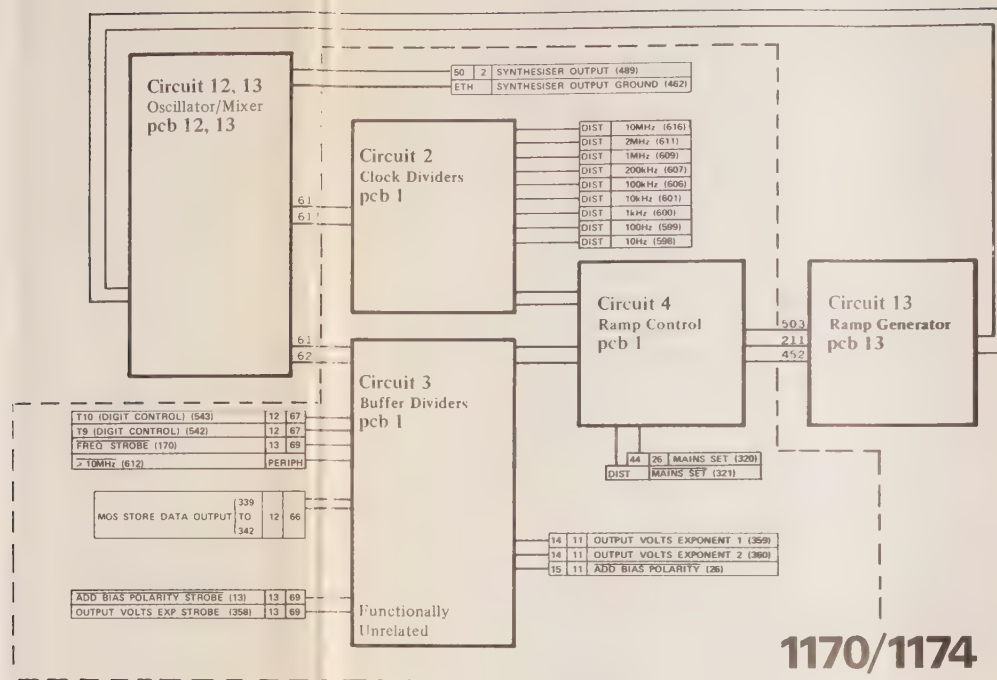


Fig. 1.3.5 SYNTHESIZER

SIGNAL GENERATION BELOW 10kHz

The GENERATOR CLOCK signal is fed to counter circuitry. During one period of the output signal, the counter fills and empties twice in a linear fashion; on the second occasion a POLARITY signal changes state. The counter digital outputs and POLARITY are converted in several stages to a constant-amplitude sinewave at the instrument operating frequency.

On ranges below 1kHz the counter is arranged to fill in 500 counts; above 1kHz but below 10kHz it fills in 50 counts. The diagram below illustrates (though for a far lower count) the counting sequence for half a period. This waveform cannot actually be observed — it is current into a virtual earth.

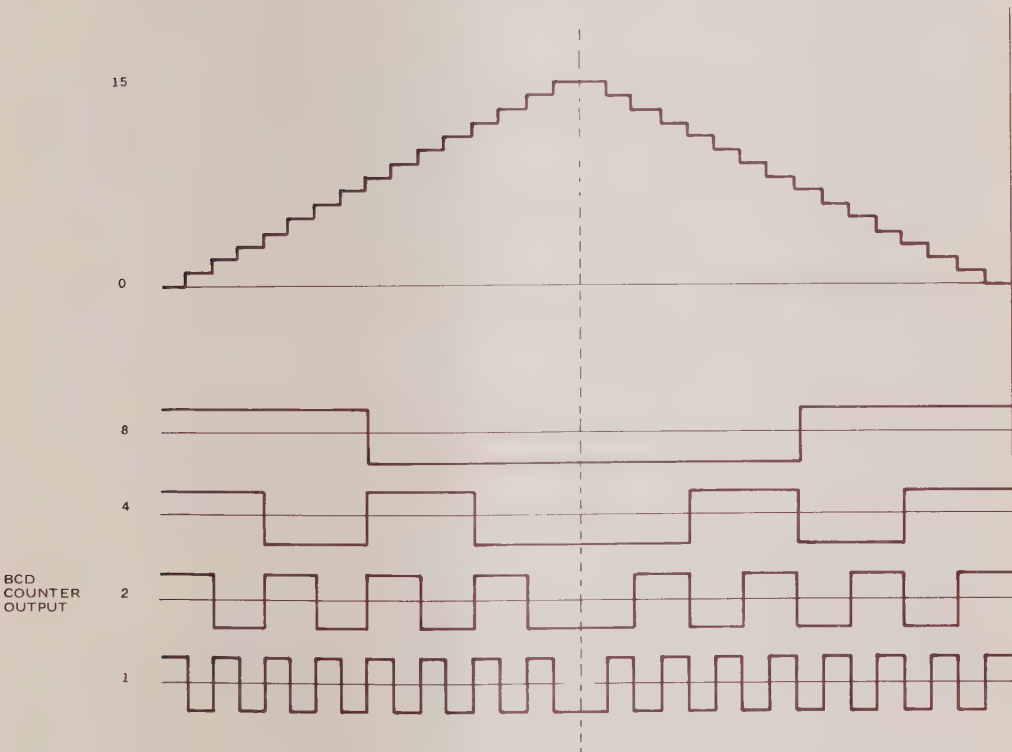


Fig. 1.3.6

SIGNAL GENERATION ABOVE 10kHz

The outputs of the “Resonant Filters” are relatively pure amplitude-controllable sinewaves, at frequencies of 10MHz and 1MHz. The V.C.O. output is divided in frequency by 2 and 20 and these are respectively mixed with the above sinewaves to give signals with nominal frequency ranges 100kHz-1MHz and 10-100kHz. The upper sidebands are filtered off and the signals are made available to the output circuitry.

THE OUTPUT CIRCUITRY

The output from the appropriate signal source is selected according to the desired frequency range. The selected signal is controlled in level by a programmable attenuator, and fed to the output power amplifier. The amplifier's low-impedance output is fed to the instrument's output connector via attenuating and protecting circuitry.

The programmable attenuator uses a d.c. control voltage which is generated as described below.

The voltage control circuit (see Circuit 19) generates analogue voltages from a digital source in circuit 72 (signal Nos. 186, 187). The system is time-shared with other parts of the instrument and comprises a signal consisting of a series of six MARK - SPACE sequences each proportional to a required analogue voltage, a RESET signal and SAMPLE signals.

Fig. 1.3.7 illustrates the facility O/PV control.

Each receiver (in this case circuit 19) shares the D/A RESET and D/A MS signals, which are used to reset an integrator and to control the time during which it ramps respectively. At a fixed time each receiver gets a unique SAMPLE signal. Each SAMPLE signal occurs at the completion of its corresponding MS signal (there are eight sequential MS signals). At this time the voltage reached by the integrator will be proportional to the sum of the mark periods. This voltage is sampled and held. It is continuously updated at each received SAMPLE signal for that particular facility.

The circuit implementation used results in the integrator ramping in a negative direction, thus the voltages which are sampled and held are negative.

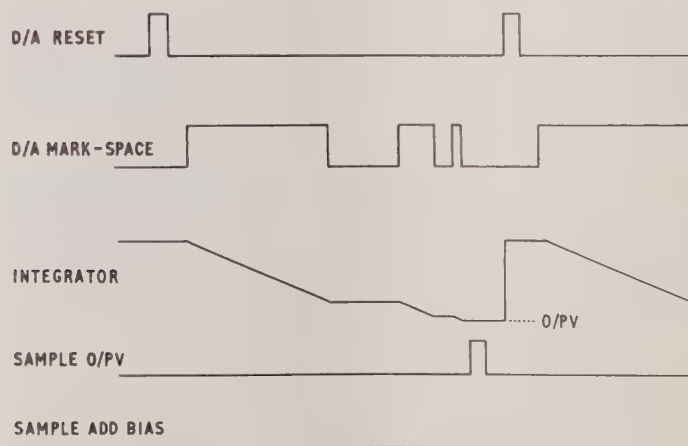


Fig. 1.3.7

THE INPUT SYSTEM

The input system comprises six circuit diagrams which may be divided into two groups. Circuits 14, 20 and 21 form the measurement circuit and circuits 22, 23 and 24 the bias reject generator.

Before attempting to understand the input system certain facts regarding the operation of the 1174 must be recapitulated. They are:-

1. A measurement is made on only one input (X or Y) at a time.
2. A voltage will be measured, and the result stored, at only a single frequency at a time. Components of the input at any other frequency will be rejected.
3. A measurement cycle consists of one or more complete periods at the measurement frequency.

MEASUREMENT SYSTEM

Measurements are made using an analogue to digital converter using voltage to frequency conversion. Fig. 1.3.9 illustrates the principle.

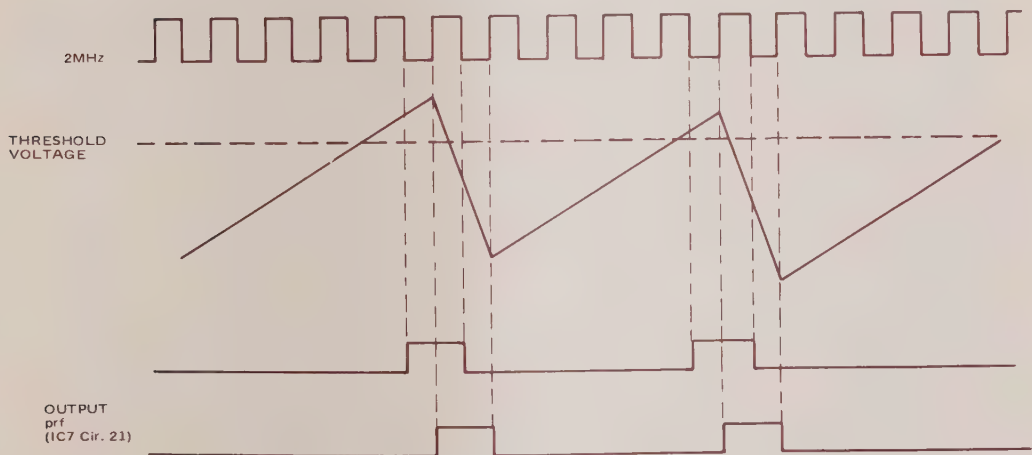


Fig. 1.3.8

The input voltage is, after suitable scaling for range, applied to an integrator, the output of which is a ramp with a slope proportional to the input voltage. When the ramp reaches a certain fixed threshold level a clock causes a pulse to be generated and the ramp to rapidly ramp down and restart. The pulse repetition frequency is therefore proportional to the instantaneous input voltage and will vary with the instantaneous input voltage over the measurement period.

A theoretical description of the use to which this pulse train is put will be found under the heading "Correlation in the 1174".

The input system, however, does far more than carry out this simple V to F operation. It also:-

1. Rejects any d.c. bias of the input signal. (Note that the 1174 inputs are a.c. coupled at operating frequencies above 10kHz and hence the Bias Reject facility need only be used below 10kHz.)
2. Reduces the frequency of signals above 1kHz by heterodyning.

The above modes of operation may be used simultaneously.

Both input modes are achieved by means of the CHOP (66) signal to circuit 21. The principle used is to change the frequency so that its fundamental component is proportional to the value to be measured.

If "bias reject" is selected a two-stage measurement operation is used. Firstly the bias is measured and secondly the signal is measured whilst a backing-off voltage, equal to the previously measured bias, is added.

As an example of the method refer to Fig. 1.3.9.

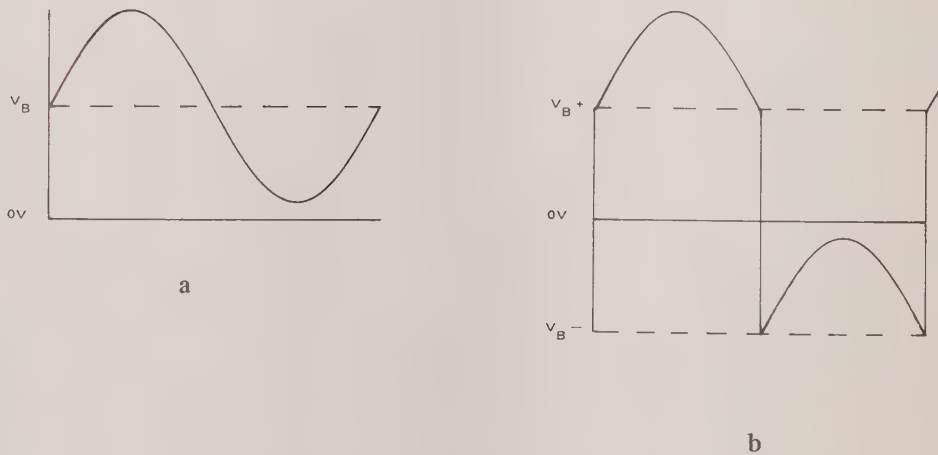


Fig. 1.3.9

Fig. a illustrates a typical input signal with bias (V_B). The FRA measures this bias by chopping the whole signal at the measurement frequency, f . The result is as shown in Fig. b. If this waveform (b) were analysed it should be found that the component at the fundamental frequency, f is proportional to the original bias voltage, V_B . The original signal voltage has, however, changed in frequency (to mainly $2f$). The 1174 will only measure the component at f , which is scaled to equal V_B .

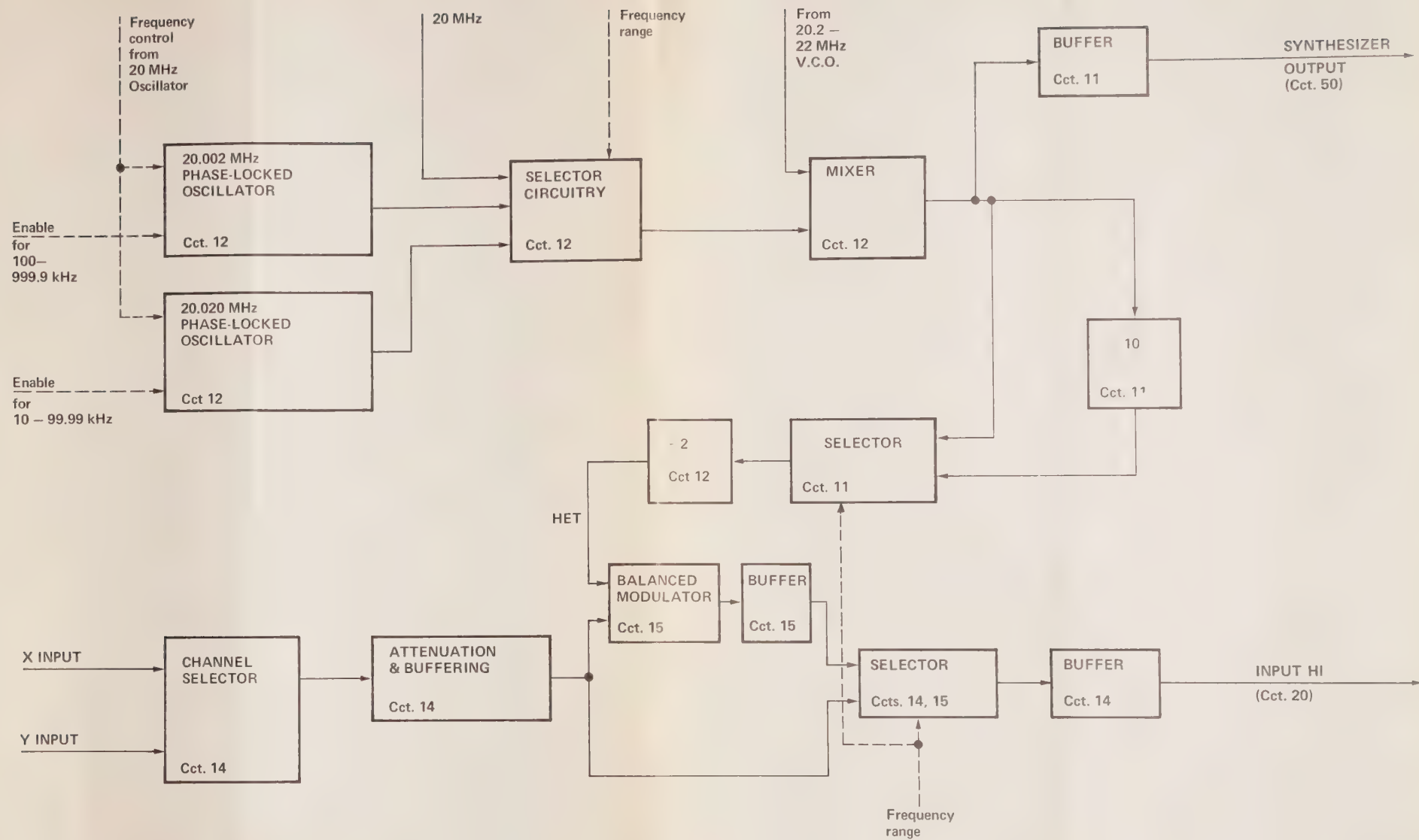


Fig. 1.3.10 1174 INPUT SYSTEM

When the FRA has finished measuring this bias voltage the measurement cycle is started. In this cycle circuits 22 to 24 are used to generate a dc voltage equal and of opposite polarity to the previously measured bias. At the same time the measurement of the signal is made with, of course, the CHOP signal removed.

(Note:- The chopping is done by switching current signals into the V to F converter, thus signals such as that illustrated above cannot actually be observed as voltage waveforms).

HETERODYNE

The FRA measures signals below 1kHz. Inputs between 1kHz and 9.999kHz are reduced before measurement by heterodyning, using the CHOP signal. The chopping frequency is, in this case, $\frac{50f}{51}$. The resulting measurement is made at $f - \frac{50f}{51} = \frac{f}{51}$.

CHOP FREQUENCY

Any combination of modes is permissible. A list of all possibilities follows, showing the com position of the chopping frequency in each case. The chopping waveform is digital and the fre quencies shown are fundamental frequencies.

CHOP (66) signal frequency

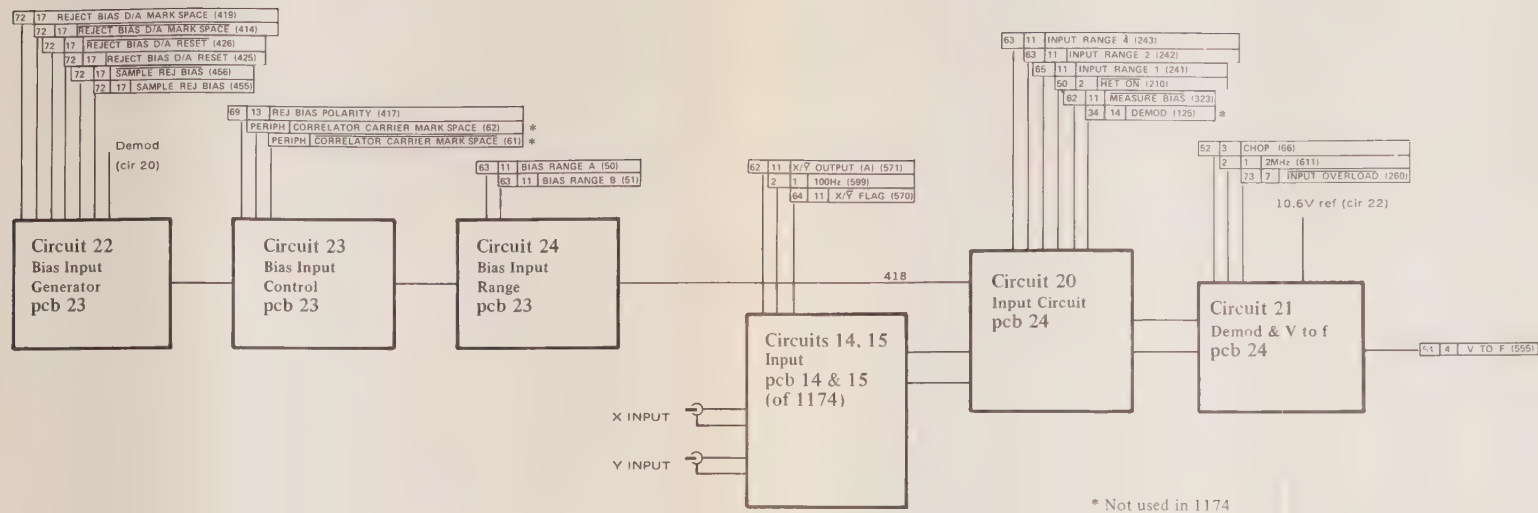
Mode	Measure Bias (1)	Measure Input
Basic	NU	N_{in}
Basic + DC Bias Reject	f	N_{in}
Basic 1kHz $\leq f < 10$ kHz	NU	$\frac{50f}{51}$
Basic 1kHz $\leq f < 10$ kHz + DC Bias Reject	f 51	$\frac{50f}{51}$ $\frac{f}{51}$

NU Measurement not made

f = Measurement frequency

Note:

- (1) This signal only exists whilst the bias is being measured, which is only for a period equivalent to the minimum integration time, at the start of each measurement.



* Not used in 1174

Fig. 1.3.11 INPUT SYSTEM

SELECTOR LATCHING

This section describes the action which takes place when a front panel touch key is touched.

Due to the complexity of the circuit not all the interconnections are shown on Fig. 1.3.12. The connections between pcb's 14 and 16 and the rest of the 1170 are shown in figure 1.3.13 which is an appendix to this diagram. Circuits 25 to 30 and 38 to 41 must be studied to find all the interconnections between them.

OPERATION

There is no direct connection between the touch key itself and the illuminating lamp. In operation, touching a key inserts data into the Latch Store in the 1170. The lamp behind the key indicates that that item of data is held in the Latch Store. When servicing this circuitry it is, of course, important to remember that these keys do not operate in the same way as a conventional illuminated push switch.

The touch keys in circuits No. 26 to 28 are scanned sequentially, in groups, by strobe pulses generated in circuit No. 25. When a touched key is detected a signal is passed to circuit 29. This bit of data will pass out of circuit No. 29 in the form of a pulse in a particular time slot of a 256 bit sequence.

The serial data are decoded in circuit 31, where instructions will be passed to insert the data into either a particular location of the Latch Store, (circuits 32 to 36) or, in the case of numerical data, to the keyboard store, (pcb 15). The keyboard store is not shown on this diagram but is included as an output of circuit No. 36. Block diagram, figure 1.3.14 shows the relationship of pcb 14 to the keyboard display system.

The output of the Latch Store is in a 4 line parallel/serial form. The first 16 time slots of the 256, used for serial data, are used to define the group of latch store data, and the 4 line parallel data the actual latch. The location of each bit of data will be found in the instructions for the use of the Store State Indicator.

The latch store output data are decoded, by use of the strobes from circuit No. 25, to illuminate the appropriate lamp, in circuits No. 38 to 41. For instance, reference to the SSI instructions reveal that the 9th time slot (address X07) contains "Sweep command" information. If at this time the value 2 (0010) is held on the 4 lines the sweep up (↑) light will illuminate.

Some of the latch store data are not carried on the 4 line bus as shown, but on separate single lines. These are shown on the individual circuits.

CIRCUITS 32 to 36

The storage devices used to hold the front panel selections are "D" type flip flops.

Data are written - in by a clock pulse which is formed by a combination of a write strobe and a data pulse. The data that is written is generated in block FLA of circuit No. 31 (D inputs to the flip-flops).

The store locations are best understood if the instructions for the use of the Store State Indicator are referred to. Table 2 of the SSI lists the Latch Store locations. The following table relates this information to the hardware.

Contents of the stores are read in sequence by the read strobes generated in block FRA of circuit 31.

Store Location	Function	Circuit		PCB	IC
		No	Block		
0 - 0	Integration time	32	FLB	14	34
0 - 1	Measure delay	32	FLC	14	34
0 - 2	Display	32	FLD	14	29
0 - 3	Measurement	32	FLE	14	29
0 - 4	Measure Sequence	33	FLF	14	36
0 - 5	Input Range	73		17	30
0 - 6	Input Range	73	—	17	30
0 - 7	Sweep Command	33	FLG	14	32
1 - 0	Sweep Mode	33	FLH	14	39
1 - 1	Keyboard	36	FLO	16	36
1 - 2	Frequency Range	35	FLM	14	42
1 - 3	Generator Mode *	35	FLL	14	42
1 - 4	Carrier Mode *	34	FLJ	14	11
1 - 5	Bias Mode *	34	FLK	14	22
1 - 6	Control	35	FLN	14	24

* Certain of these facilities are not used by the 1174.

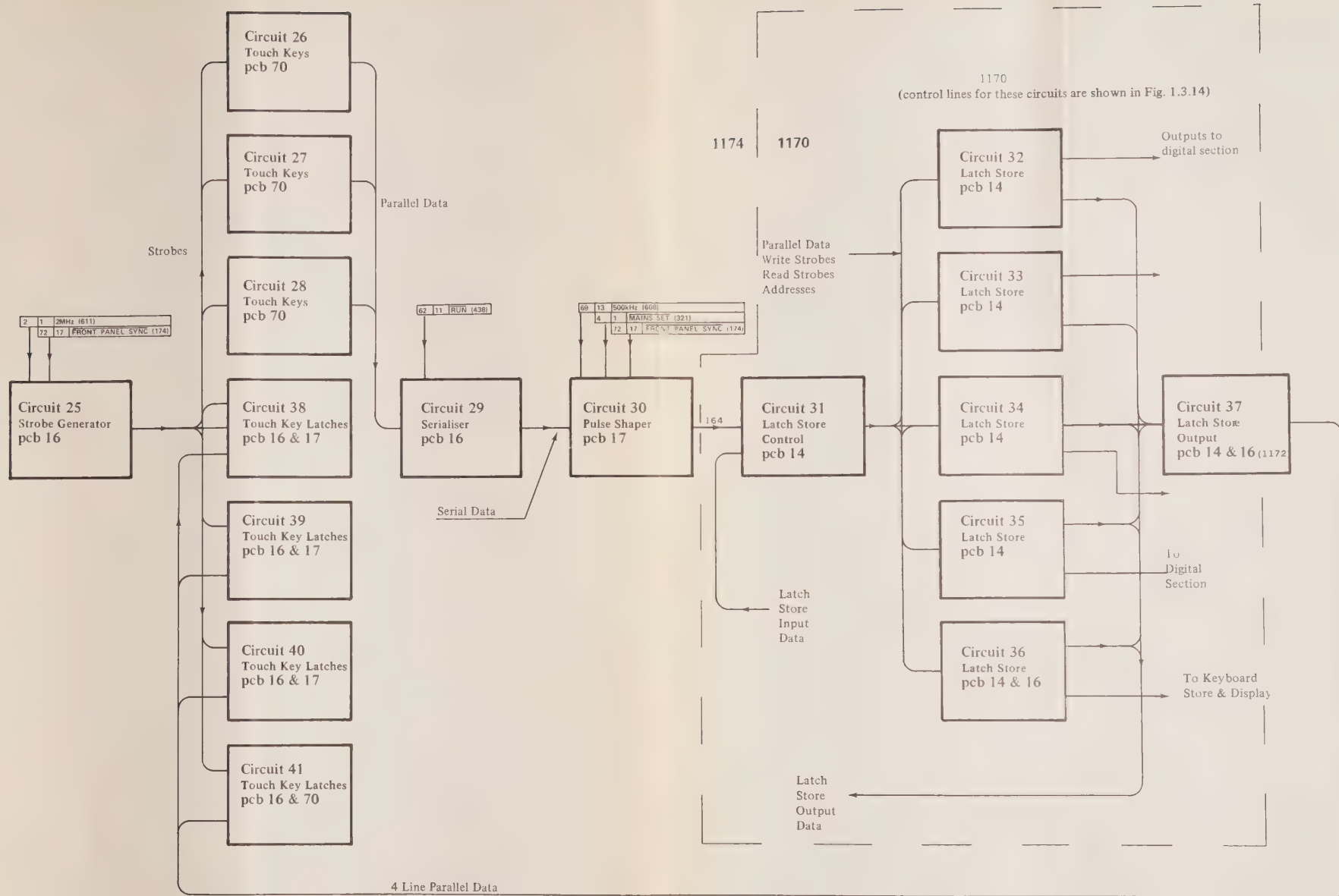
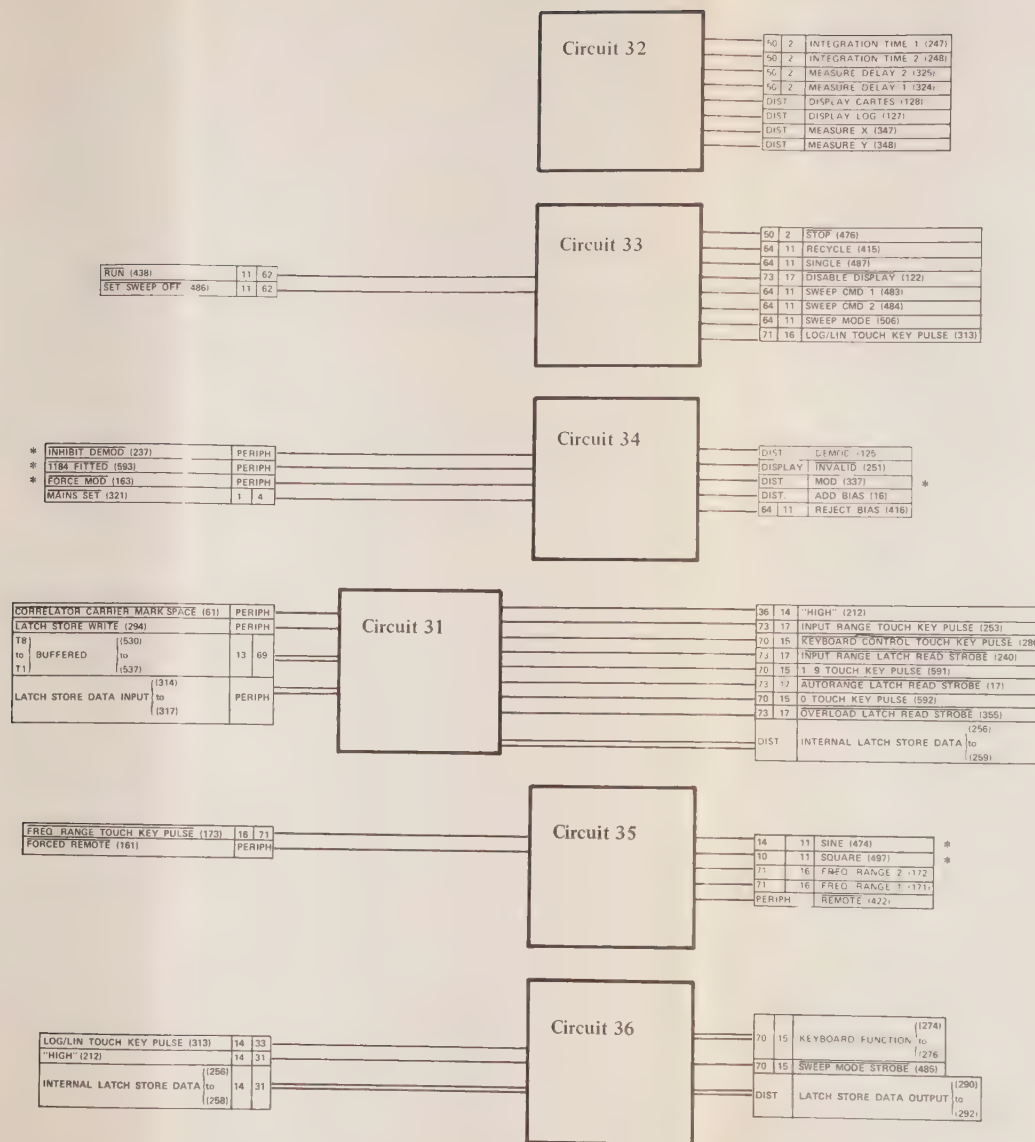


Fig. 1.3.12 SELECTOR LATCHING



This diagram which is an extension of Fig. 1.3.13 shows the details of connections to circuits 31 to 36.

Fig. 1.3.13

LATCH STORE CONTROL LINES

* Not used in 1174

DIGITAL SECTION - MAIN STORE AND DISPLAY

This diagram should be examined in conjunction with that of the arithmetic unit. The main store, pcb 12, is common to the two diagrams and is the heart of the digital section.

Due to the complexity of interconnection and the type of signals involved, it is not normally possible to trace signal paths through this section. The paths shown must therefore be regarded as theoretical associations between circuits and not actual connections. The purpose of the diagram is to assist in locating a fault to the pcb involved rather than the faulty component.

OPERATION

The main store (pcb 12) contains all the numerical data used and displayed in the 1170. A complete list of these data is given in the instructions for the use of the Store State Indicator (special test equipment type TG1212A).

Data are read from the store in many different ways but the general paths are shown on this diagram. Circuit No. 69, pcb 13 is used as an addressing system for the main store data, which is directed to the locations shown.

Part of this diagram is an extension of the Selector Latching diagram. The touch keys are shown connected to circuits 70 and 71. In fact this line represents keyboard data keyed in from the numerical touch buttons and is inserted via circuits 29, 30, 31 and 36. The data are held in the keyboard store until the ENTER key is touched, when they are entered into the MOS (main) store.

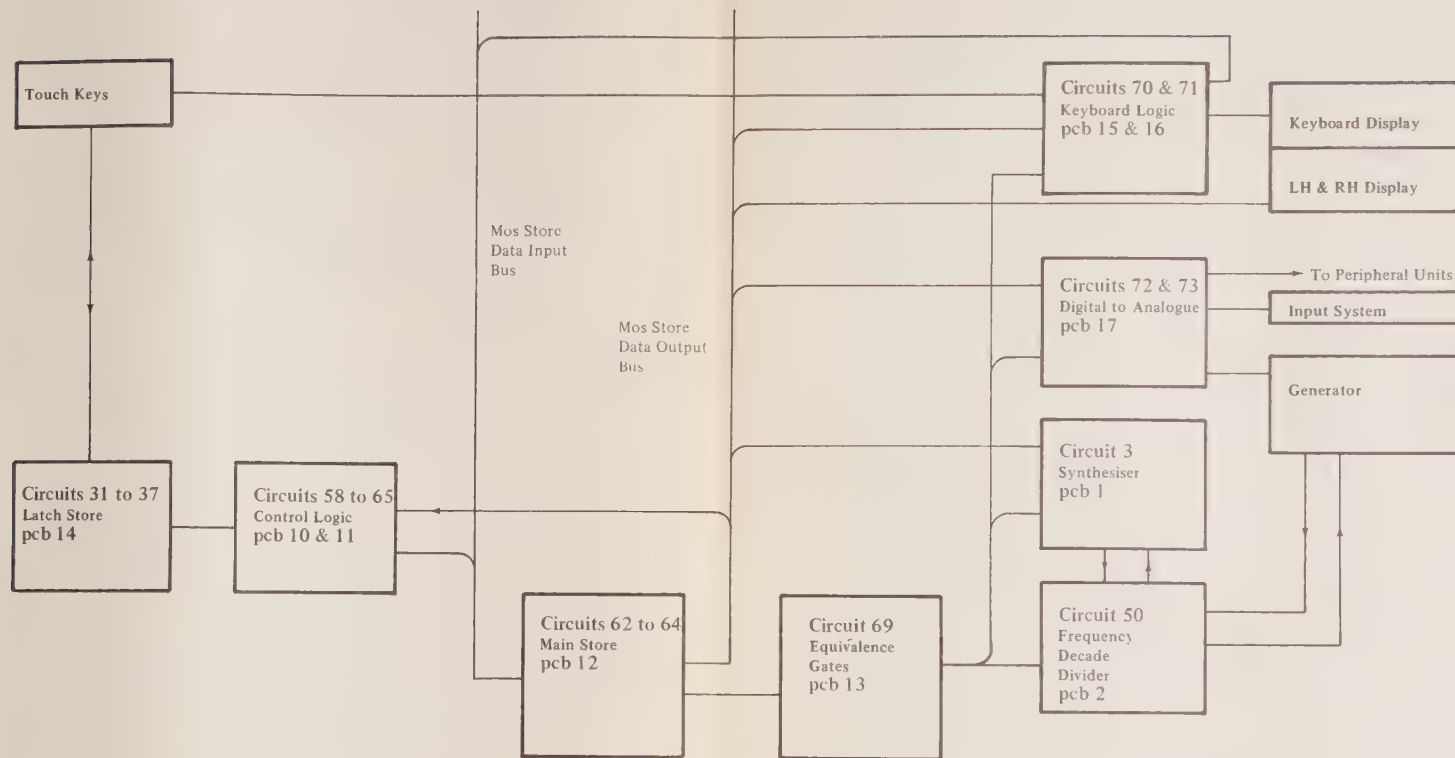


Fig. 1.3.14
DIGITAL SECTION, MAIN STORE
AND DISPLAY

DIGITAL SYSTEM - ARITHMETIC UNIT

This diagram should be examined in conjunction with that of the Main Store and Display. Like that diagram this contains information regarding associations between circuit diagrams and pcb's and not actual connections between them.

A theoretical and mathematical description of this section is given from page 1.3.31.

As can be seen from this and its associated diagram, information is received from many sources into the arithmetic unit and, after processing, is deposited in the main store, for further processing or display.

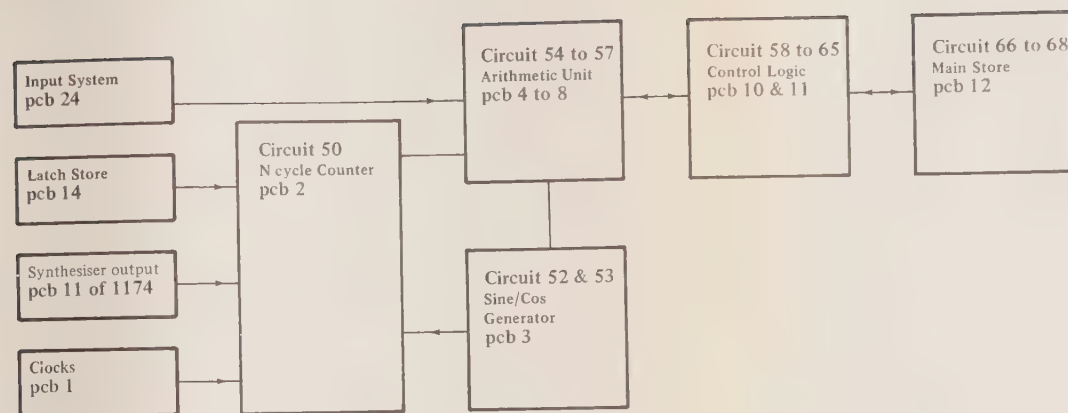


Fig. 1.3.15

DIGITAL SECTION - ARITHMETIC UNIT

CORRELATION IN THE 1174

INTRODUCTION

The 1174 is a “**Frequency Response Analyser**”. It is usually used to measure the response of a system to a sine wave stimulating signal over a range of frequencies. Normally the stimulating signal is the output of the 1174 generator, a sine wave at frequency f .

The output of the system on test, can be split, by means of Fourier analysis, into a fundamental response (a sine wave at frequency f), harmonics (sine waves at integral multiples of frequency f) due to the non-linearities in the system on test, and any non-harmonically related noise. The 1174 measures the *fundamental* sine wave response, ignoring as far as possible any harmonics or random noise present. It is resolved into two components - one due to a sine wave IN-PHASE with the generator output, and one due to a sine wave in QUADRATURE with the generator output. This enables the PHASE response of the system to be measured as well as the AMPLITUDE response.

Measurements made over a range of frequencies enable the system frequency response, in phase and amplitude, to be built up.

BASIC PRINCIPLES

The 1174 uses a correlation process to measure the in-phase and quadrature components of the fundamental response of the system. Operation of the correlator in its basic mode will be assumed in the description below.

The generator output is a signal of the form $v_G = A_G \sin 2\pi ft$.

The output of the system on test is a signal $v_c(t)$.

To calculate the in-phase component at frequency f , this signal is multiplied by a signal $\sin 2\pi ft$, and integrated with respect to time, for a whole number of cycles N . This gives the result:

$$I_A = \int_0^T v_c(t) \sin 2\pi ft \, dt \quad \text{where } T = \frac{N}{f}$$

Similarly the quadrature component is calculated by forming the integral,

$$I_B = \int_0^T v_c(t) \cos 2\pi ft \, dt$$

If the components of $v_c(t)$ are $A \sin 2\pi ft$ (in-phase) and $B \cos 2\pi ft$ (quadrature) respectively, then:

$$\begin{aligned} I_A &= \int_0^T (A \sin^2 2\pi ft + B \sin 2\pi ft \cos 2\pi ft) \, dt \\ &= \frac{1}{2}A \int_0^T (1 - \cos 4\pi ft) \, dt + \frac{1}{2}B \int_0^T (\sin 4\pi ft) \, dt \\ &= \frac{1}{2}AT - \frac{1}{2}A \int_0^T \cos 4\pi ft \, dt + \frac{1}{2}B \int_0^T \sin 4\pi ft \, dt \end{aligned}$$

For a whole number of cycles, the integrals in this expression are both zero, hence:

$$I_A = \frac{1}{2}AT.$$

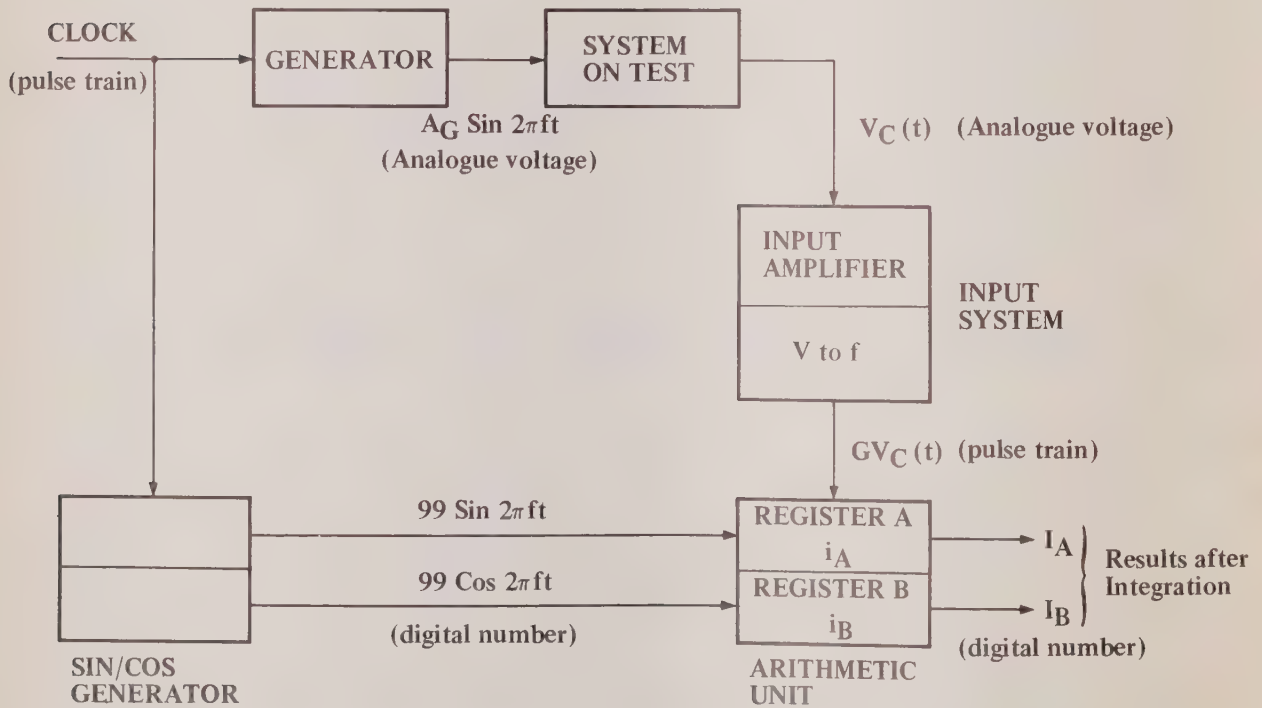
$$\text{Similarly, } I_B = \frac{1}{2}BT$$

Division by time of integration, T , allows the amplitudes of the in-phase and quadrature components, A and B , to be determined.

It can be shown that this method rejects harmonic components of $v_C(t)$ completely, and gives good rejection of random noise, which can be further improved by lengthening the integration time, T .

THE MECHANISM OF CORRELATION

The correlator contains a "sin/cos generator" (board 3), which produces the values of $\sin 2\pi ft$ and $\cos 2\pi ft$ necessary for the correlation process. The outputs of the sin/cos generator are two signed 2 digit BCD numbers, each in the range +99 to -99, equal to $99 \sin 2\pi ft$ and $99 \cos 2\pi ft$. The "sine" value is fed to arithmetic register A (board 5) and the "cosine" value to register B (board 6). These numbers are always available to the arithmetic unit, and follow the generator output sinewave.



CORRELATION IN THE 1174

The output of the system on test, $v_C(t)$ is applied to the correlator input terminals. It then enters the input system (boards 23 & 24), which consists of an input amplifier and a voltage to frequency converter (V to f), with an overall system gain of G pulses per second per volt.

The output of the V to f ($Gv_C(t)$ pulses per sec.) is fed to the arithmetic unit (board 4). On receiving each V to f pulse from the input system, the arithmetic unit adds the current value of "sine", presented to it by the sin/cos generator, to the contents of register A. Likewise, the current value of "cosine" is added to the contents of register B.

If the instantaneous contents of register A are i_A , and of register B are i_B , the rates of increase of the contents of the register are given by:

$$\frac{di_A}{dt} = Gv_c(t) \cdot 99 \sin 2\pi ft \quad \text{and} \quad \frac{di_B}{dt} = Gv_c(t) \cdot 99 \cos 2\pi ft$$

The final contents of the registers after the integration process are given by

$$I_A = \int_0^T Gv_c(t) \cdot 99 \sin 2\pi ft \, dt \quad I_B = \int_0^T Gv_c(t) \cdot 99 \cos 2\pi ft \, dt$$

These results, with a suitable scaling factor, allow the in-phase and quadrature components of the system fundamental response to be calculated (see the explanation of the correlation process, above).

MODES OF OPERATION OF THE CORRELATOR

The sin/cos generator input to the arithmetic unit represents a sine wave at a certain frequency (the "correlator frequency"). The V to f signal is derived from the signal present on the analyser input terminals. The characteristics of the correlation process ensure that only the component of this V to f signal which is at the correlator frequency contributes to the result. If the correlator frequency is different from the frequency of the component of the input signal which is to be measured (the "measuring frequency"), the input system must change the frequency of the input signal before it reaches the V to f, so that the desired component will be correlated.

(a) Basic Mode

The basic mode of the correlator is used for measuring frequencies below 1kHz. In this mode, the correlator and the generator operate at the same frequency f . The frequency of the generator output sine wave is determined by the frequency of a clock signal (the "generator clock") which contains 2000 pulses for each cycle of output sine wave. The generator clock is thus at a frequency $2000f$. This is divided by ten to produce the clock ($200f$) for the sin/cos generator, which always requires 200 pulses for each cycle. The sin/cos generator output thus represents a signal at frequency f , locked to the generator. The input system does not alter the frequency of the input signal, so the component at frequency f is measured.

GENERATOR
CLOCK

2000f

GENERATOR
< 10kHz

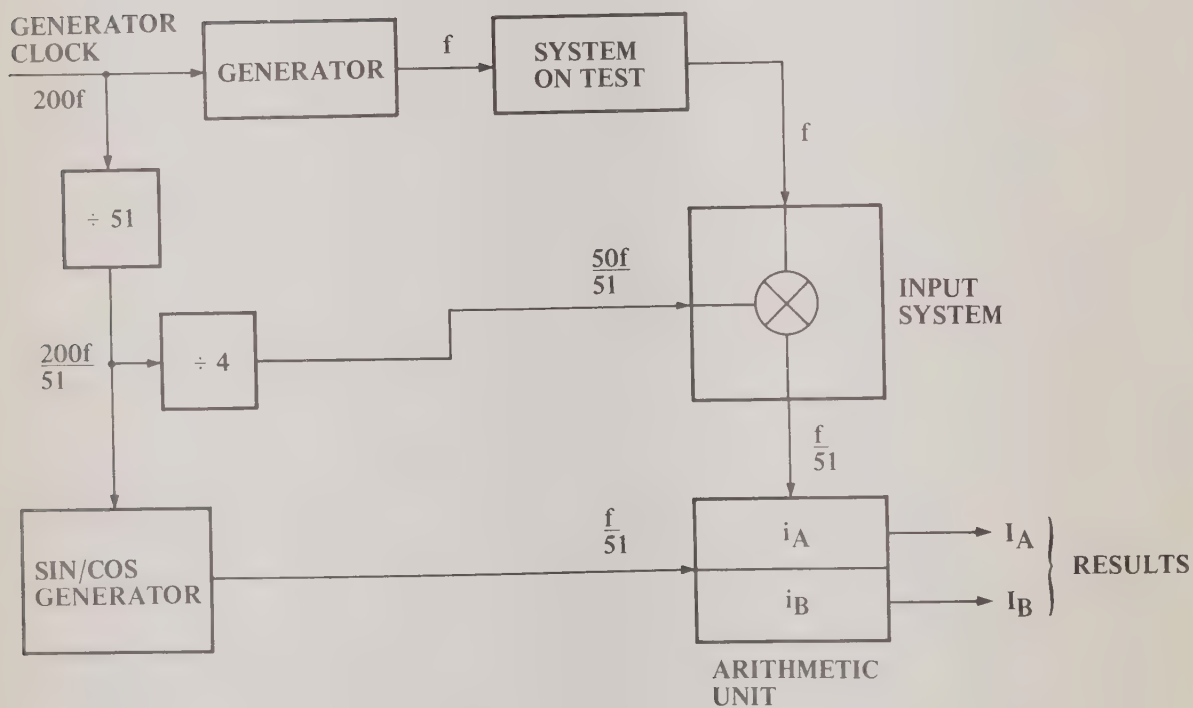
f

SYSTEM
ON TEST

f

(b) Heterodyne Mode

The correlator is capable of giving accurate results only up to a frequency of 1kHz. At measuring frequencies from 1kHz to 9.999kHz, the correlator operates at a lower frequency, enabling accuracy to be maintained. On this frequency range, the generator only requires 200 pulses per cycle. The generator clock is at frequency $200f$. It is divided by 51 to produce the clock for the sin/cos generator ($200f/51$). The sin/cos clock is also divided by 4 to give a heterodyning signal at frequency $50f/51$. The input system multiplies the input signal by this heterodyning signal, to produce a difference signal at the correlator frequency, $f - 50f/51 = f/51$.

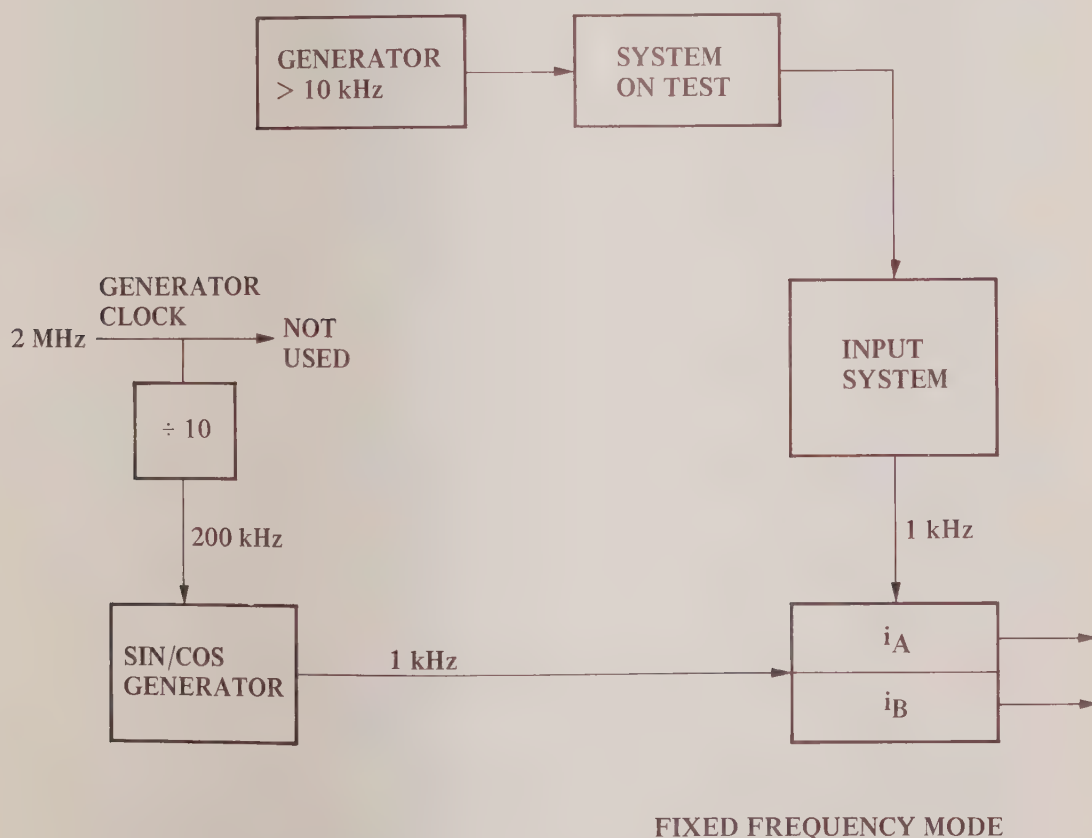


HETERODYNE MODE

(c) Fixed Frequency Mode

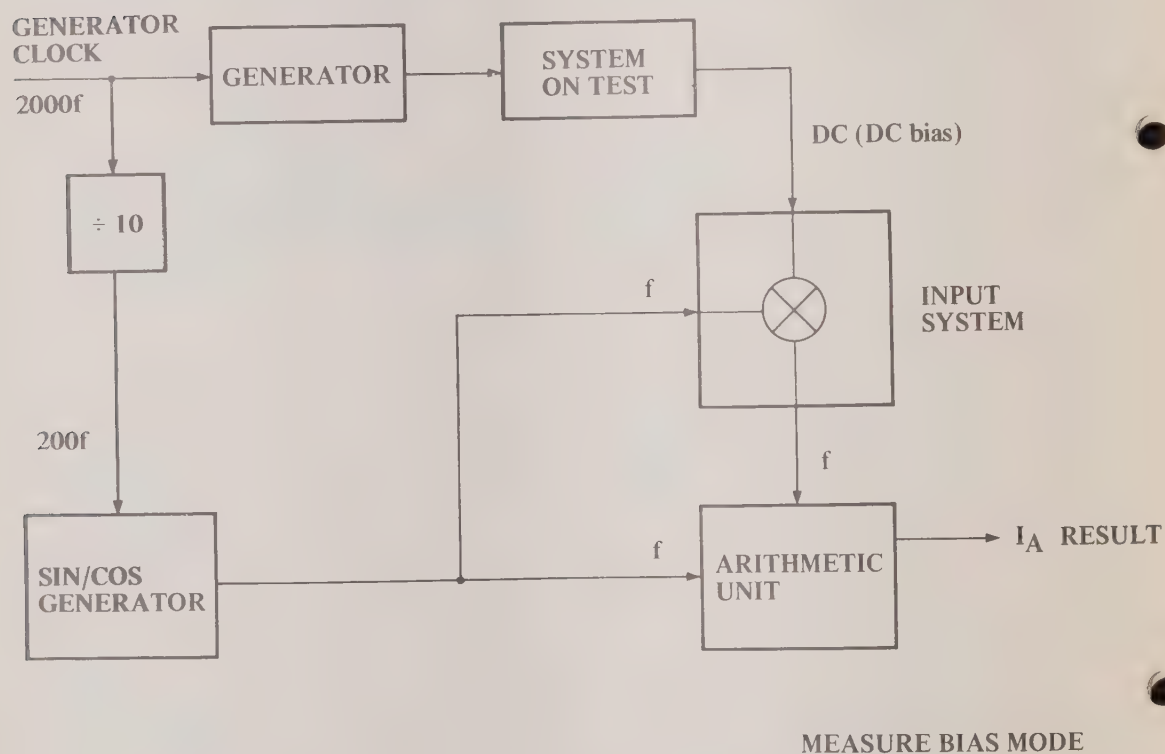
The correlator is only capable of working accurately at frequencies up to 1kHz. The 1kHz-9.999kHz range is taken care of by heterodyning; the two top frequency ranges work in yet another way. Operation on one of the two top frequency ranges is detected (within Circuit 50) and a fixed clock of 2MHz is put on the GENERATOR CLOCK line instead of a clock of 2000f pulses/cycle. (Note that the GENERATOR CLOCK is not used to produce the generator output on these ranges, as has been explained in "Introduction to the Generator".) This is then divided in frequency by ten as in the Basic Mode to give 200 pulses/cycle at a constant correlator frequency of 1kHz.

The 1174 input circuitry is arranged on the two top ranges to heterodyne components in the input signals at the instrument output frequency down to a fixed 1kHz and thus these may be correlated in the normal way.



(d) Measure Bias Mode

When "Reject Bias" is programmed, the correlator is used to measure the DC voltage on the input terminals, so that a "backing-off" voltage can be generated. This measurement is made in the "Measure bias" mode. The input to the correlator is multiplied by a square wave at the correlator frequency f . This converts any DC present to AC at frequency f , which is then correlated. (The "signal" present at the input terminal is converted to a mixture of DC and harmonics, all of which are rejected by the correlator, and thus does not interfere with the bias measurement).



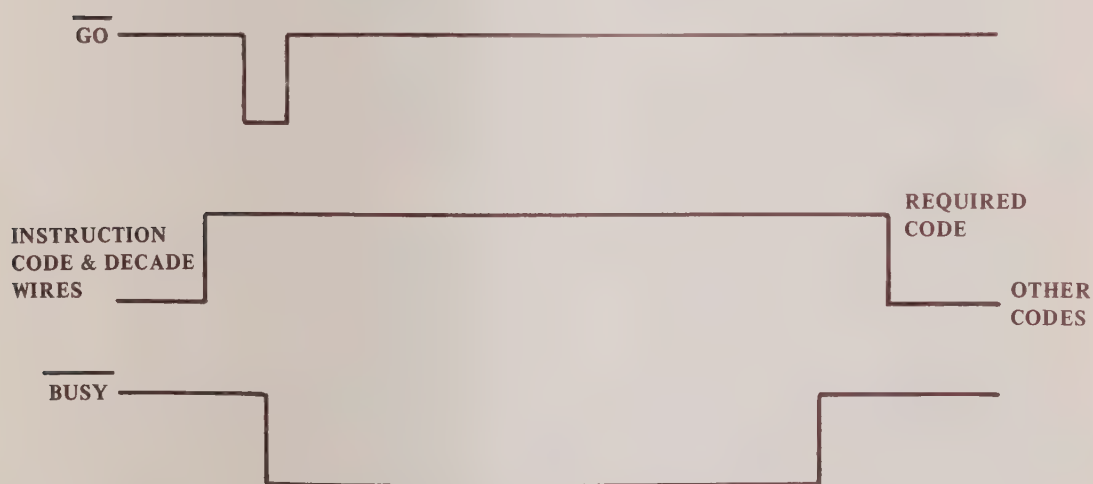
(e) Combinations of modes

It is only possible (and necessary) to measure bias on frequency ranges below 10kHz, since the inputs are a.c. coupled above this frequency. For frequencies between 1 and 9.999kHz the output from the system under test is not multiplied by the heterodyning signal when measuring bias, as this is not necessary.

INTRODUCTION TO ARITHMETIC UNIT

The arithmetic unit is capable of performing 32 different operations. Some of these transfer information to or from the store. Some are simple calculations, such as an addition, and some are more complex, such as calculating the logarithm of a number. The most complex operation which can be performed autonomously by the arithmetic unit (in conjunction with the input system, the sin/cos generator and the N-cycle counter) is the correlation process itself (the operation performed by the arithmetic unit during the correlation process is termed "integration"). More complicated calculations are made up of sequences of instruction, which are commanded in turn by the control logic.

The control logic produces a 6 wire instruction code to the arithmetic unit. Five of these wires specify which of the 32 instructions the arithmetic unit is to perform. When the code has been set up, the control logic issues a $\overline{GO}$ pulse to the arithmetic unit, which is the command to start the specified operation. When the $\overline{GO}$ pulse has been accepted, the arithmetic unit returns a $\overline{BUSY}$ signal to the control logic. This inhibits further control logic action until the arithmetic unit operation is completed. The arithmetic unit then performs the operation. This may take $2\mu\text{Sec}$ for a single addition, or several hours for a long integration. When it has finished it removes the $\overline{BUSY}$ signal to the control logic, which then continues to the next instruction in the program.



Arithmetic Unit Command Sequence

Some arithmetic unit operations make use of a decade number. This is produced by the control logic before the $\overline{GO}$ pulse, as a 3 wire binary number.

After an arithmetic unit operation, the control logic can use conditional instructions to sense various conditions in the arithmetic unit.

The arithmetic unit communicates data via a 4 wire static data bus. This allows it to transfer 4 bit numbers between registers within itself, or to and from the store. When communicating with the store, data is transferred between the arithmetic unit data bus (static) and the store data bus (dynamic i.e. changing every $2\mu\text{Sec}$) by an interface on Board 11, which is controlled by the control logic. Three "enables" wires, which are produced by the control logic, control which of the three registers in the arithmetic unit is allowed to write onto the data bus.

The signals described are sufficient for the arithmetic unit to perform any of its 32 operations except for integration (and measure delay), which is described later.

ARITHMETIC UNIT INTERNAL ORGANISATION

The arithmetic unit proper (excluding parts used only for integration and measure delay) consists of the following parts:

- 1. Decode Logic
Translates 5 instruction code wires from the control logic into the 22 wires necessary to control the individual parts of the arithmetic unit. (These wires are all static throughout an operation)
- 2. Condition Multiplexer
Used to feed information about the contents of the registers etc. to the control logic.
- 3. Sequence Logic
Receives the $\overline{GO}$ pulse from the control logic and generates all sequential pulses and clocks required by the various parts of the arithmetic unit. A $\overline{BUSY}$ signal is returned to the control logic to prevent it continuing to the next instruction until the current one has finished.
- 4. Registers A & B
Both registers are identical. Each stores a 9 digit BCD number, with sign, and is capable of adding or subtracting another 9 digit number from it, in $1.8\mu\text{Sec}$.
- 5. Register C
This is also referred to as the iteration counter or timer counter. It is a 6 digit BCD up/down counter. The i/p clock can be applied to any of its 6 stages, thus changing the significance of each i/p pulse.
- 6. Exponent Counters
Exp A and Exp B are 4 bit counters, used to keep the exponents of the contents of register A and B during shift operation etc. They can be read by, or loaded from the store, via the data bus. An Exp C is also available and can be read by the store (it cannot be loaded). It is always equal to $\text{Exp B} - \text{Exp A}$.

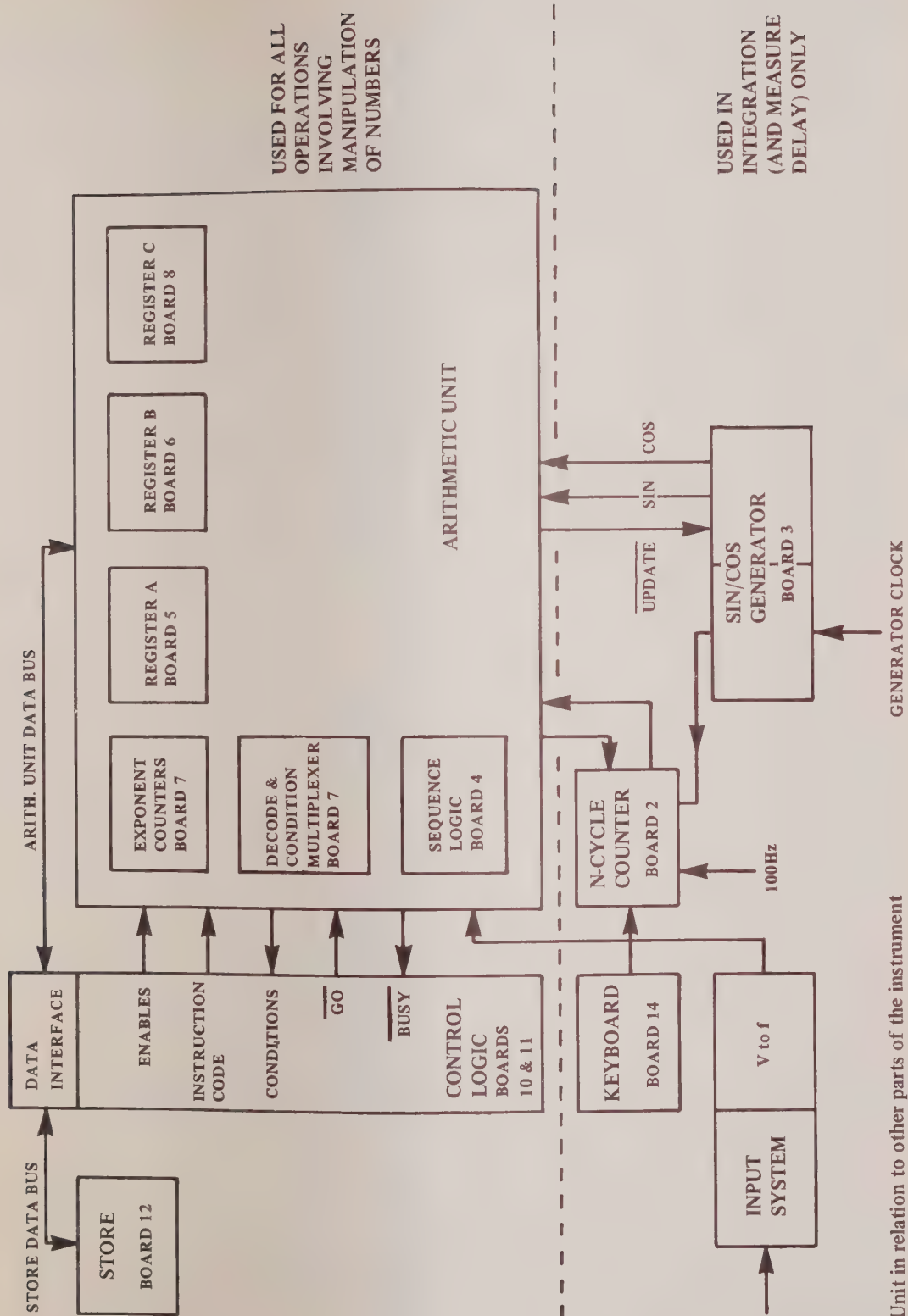
The arithmetic unit operates in "cycles". Each cycle takes $1.8\mu\text{Sec}$. Some arithmetic unit operations take only one cycle (e.g. an addition or a transfer of one digit between a register and the data bus), others may take up to 2 or 3 thousand cycles (e.g. calculating a logarithm) whilst integration may take a more or less unlimited number of cycles.

Registers A and B can each store a 9 digit BCD number, and a sign, indefinitely. The most significant digit is an overflow digit, and is known as the 9th digit. The remaining digits are numbered from 0 (most significant, except for the 9th digit) to 7 (least significant). In a single cycle, either or both registers can add or subtract another 9 digit number (the "input data") from the current contents of the register. The answer becomes the new contents. More complex operations are made up of many such cycles, each consisting only of additions or subtractions. Each register can select one of a number of sources from which the input data may come. Each register produces 3 output signals which may be used as input data either by itself or by the other register. The outputs are equal to:

(a)	the register contents	A	B
(b)	the register contents $\times 10$	10A	10B
(c)	the register contents $\div 1000$	A/1000	B/1000

Input data may also come from other sources (data bus, sin/cos generator, or log constant from board 4). The registers may add none, some or all of the 9 digits of the input data. The number may be added to the current register contents, or the current contents may be discarded and the input data added to zero. Different combinations of these alternatives produce all possible types of cycle which the arithmetic unit can perform.

The various cycle types are described in Table A.



Arithmetic Unit in relation to other parts of the instrument

REGISTER A				REGISTER B							
SEE NOTE NO.	DIGITS OF INPUT DATA ADDED 9th 0 1 2 3 4 5 6 7	ADD/SUB	SOURCE OF I/P DATA	ADDED TO	ADD/SUB	SOURCE OF I/P DATA	DECADE NO.	INSTRUCTION NAME	CODE	NOTES	
1,11			Zero	Current conts.		Zero		Read	12	Also used for CLoad, AExp dec, BExp dec	
2			Zero	Zero	+	Register B		AClear	8		
2		+	Register A	Zero		Zero		BClear	9		
3			Zero	Current conts.	+	Register A		BAdd	0		
3			Zero	Current conts.	-	Register A		BSub	1		
3		+	Register B	Current conts.		Zero		AAdd	2		
3		-	Register B	Current conts.		Zero		ASub	3		
4		+	Register A	Current conts.		Zero		ADouble	19		
4			Zero	Current conts.	+	Register B		BDouble	20		
5		+	Register B	Zero	+	Register A		Swap	21		
6		-	Register A	Zero	+	Register B		AInv	17	Subtracts Register A from zero, forming 10s complement	
7			Register A	Zero		Register B		Complement	18	Subtracts either register from zero if it is negative	
8		+	10A	Zero	+	Register B		ATen	29	Shifts register A one decade up	
8		+	Register A	Zero	+	10B		BTen	30	Also used for CTen. Shifts register B one decade up	
9		-	10A	Current conts.		Zero		Ax-9	16	Multiplies register A by -9	
10		+	Data bus	Current conts.		Zero	0	ALoad	10	Also used for AOne load	
							1				
							2				
							3				
							4				
							5				
10			Zero	Current conts.	+	Data bus	0	BLoad	11	Also used for BOne load	
							1				
							2				
							3				
							4				
							5				
12		-	Log const.	Current conts.	+	B/1000		Log	4		
13		+	Log const.	Current conts.	-	B/1000		Exp	5		
14		+	B/1000	Current conts.	-	A/1000		Polar	6		
15		-	B/1000	Current conts.	+	A/1000		Cartes	7		
16			Zero	Current conts.	-	Register A		XDivide	22	} Iterative operations (10 cycles max) used in the division routine.	
16			Zero	Current conts.	+	Register A		YDivide	23		
17			Zero	Current conts. ÷ 10		Zero		DTen	26		Shifts both registers one decade down.
18 {			Sin "1" digit	Current conts.		Cos "1" digit		} Int	24		
			Sin "10" digit	Current conts.		Cos "10" digit					

The ADDED TO column refers to both registers. The contents of register A after an operation is the sum (or difference) of the SOURCE OF INPUT DATA (Reg A) column and the ADDED TO column. Thus for AAdd, the contents of register A after the operation is Register B + Current conts of Register A. Similarly for register B.

The DIGITS OF INPUT DATA ADDED column shows which digits of the input data are added to (or subtracted from) the register. Thus the data bus is added to one digit only, in a Load operation, and the least significant 6 digits only of the B/1000 signal are used in a Log operation.

NOTES

SINGLE CYCLE OPERATIONS

1. Registers A & B are each equipped with an “output latch”, which is used when a digit is read from the register onto the data bus. Digits 0 to 5 may be read onto the bus. If one of these is selected by the “decade” wires (from the control logic), it is entered into the output latch during any cycle performed by the arithmetic unit, of whatever type. The contents of the latch are read onto the data bus when the “enable” wire (from the control logic) for the register is high. Normally the sequence to read a digit consists of setting up the decade wires to the desired digit number, performing a “read” operation in the arithmetic unit, and enabling the register which is to be read. The desired digit is then present on the data bus and may subsequently be loaded into another register, or the store.

The “read” operation does not alter the contents of either register. Its function is to ensure that the desired digits are entered into the output latches.

It is also used for certain auxiliary operations which affect only the exponent counters or register C. Signs and exponents, and data in register C, are read onto the data bus immediately their decade number and enable wire are set up (i.e. they do not require a cycle to “latch” them). However, for the sake of uniformity, a “read” operation is normally performed as for digits 0 to 5 of registers A and B.

For the purpose of communication via the data bus the signs are allocated decade number 6 (+ve = value 0, -ve = value 1) and exponents decade number 7.

2. **Clear operations** clear all 9 digits of the register in question to zero. The signs and exponents are unaffected by a clear operation. In order to clear them it is necessary to load zero into them from the data bus. This is also true of register C (there is no CClear operation).

3. **Additions and subtractions** are single cycle operations. They are full 9 digit calculations. Carries and borrows out of the 9th decade are lost. The sign bistables will follow changes of sign correctly only if negative numbers are in 10's complement form before the addition or subtraction. Answers will then also be in 10's complement form if negative. If the signs are not of interest, additions and subtractions may be performed on numbers in “absolute value and sign” form - the operation will take place on the absolute values, the result will be complemented if the difference in absolute values (in a subtraction) was negative, and the signs will not have any straightforward meaning after the operation.

4. **“Double” operations** are performed by adding the number to itself. Signs are unaffected, and carries out of the 9th decade are lost.

5. **A “Swap” operation** adds the contents of register A to register B, and the contents of register B to register A. The input data is added to zero in each register. Signs and exponents are unaffected (i.e. they are NOT swapped).

6. **An “AInvert” operation** subtracts the contents of register A from zero. Register B and both signs are unaffected.

7. **Complement.** The register are set up as if they were each to subtract their current contents from zero. However, gates on boards 5 and 6 ensure that they are subtracted if negative, and added if positive. The 10's complement is thus formed. Signs are unaffected. This operation is used to convert numbers in “absolute value and sign” form to 10's complement form and vice versa.

8. **ATen, BTen, and CTen operations** add the current contents x10 to zero in one register, the the contents of which are thus shifted up one decade, and add the contents to zero in other register, which is thus unaffected. The 10A and 10B signals are formed by a circular shift process, so that the 9th decade of the contents of register A becomes digit 7 (least significant digit) of signal 10A. Signs are unaffected by the operation. In ATen and BTen operations, the exponent of the register being shifted is reduced by one, to keep the magnitude represented by the register constant. Exponents are not affected by CTen (this is the only difference between BTen and CTen).

9. The **Ax-9** operation subtracts $10A$ from A , giving a result $-9A$. In conjunction with **AInvert**, this enables numbers to be multiplied by 9, which is useful in calculating degrees from radians. Register B , signs and exponents are unaffected by the operation.

10. **ALoad and BLoad**. These operations add the data present on the data bus to the register, in one digit position only between 0 and 5. It is not necessary for the register to contain zero before the operation - input will be added correctly (loading of register A and B is additive). If digits 6 (sign) or 7 (exponent) are addressed, the contents of the register will remain unchanged, but the data present on the data bus will replace the current contents of the sign bistable or the exponent counter of the register in question (loading of signs and exponents is destructive). The 9th digit 6 and 7 of the registers themselves cannot be loaded from or read onto the data bus.

11. **CLoad**. One of digits 0 to 5 of register C may be loaded from the data bus by a **CLoad** operation. This is accompanied by a "read" operation which has no effect on the contents of register A and B . Loading of results C is *destructive* - no **CClear** operation is provided. If digit 6 or 7 is addressed, the **CLoad** operation has no effect at all.

ITERATIVE OPERATIONS

Outputs are provided from registers A and B to show when a carry or borrow from digit 0 into the 9th decade has occurred. An output is provided from register C to show when it has counted to state zero, either by overflowing (when counting UP) or by counting DOWN to zero. Circuitry is provided (Board 4) so that when commanded to "go" by the control logic, the arithmetic unit will perform cycles continuously until one of the above three things happens. The arithmetic unit then returns control to the control logic by removing the **BUSY** signal. Counting to zero in register C will always terminate an iterative operation. Some iterative operations are also terminated by a carry or borrow in either register A or register B .

12. **Log**. In a cycle of a "log" operation, $B/1000$ is added to the current contents of register B . This has the effect of multiplying the contents of register B by 1.001. A constant (log const.) equal to $\log 1.001$ ($= .00043402$) generated on board 4, is subtracted from register A .

Since the $B/1000$ signal is generated by a circular shift process, the least significant three digits of B appear as the most significant 3 digits of $B/1000$, which should all be zero. Therefore in operations involving the $B/1000$ and $A/1000$ signals, only the least significant 6 digits of the input data are added to the registers.

The log operation commences with the number whose log is to be found in register B . Its most significant digit must be in digit 0 position (i.e. the number must be "normalised"). Register A contains zero, or a digit in the 9th decade only. Cycles of the type described above are then executed continuously until the signal indicating a carry into the 9th decade of register B appears. When this is received by the sequence logic (Board 4) it terminates the operation and removes the **BUSY** signal to the control logic, which continues to the next instruction in the program.

If we treat the decimal point of the registers as being between the 9th decade (integer part) and the rest of the register (fractional part), then the function of the log operation is to determine how many times it is necessary to multiply the initial value B ($1 > B \geq .1$) by 1.001 in order to make it ≥ 1 . This number is equal to the number of cycles performed, N .

This gives:

$$1 \approx B \times 1.001^N$$

$$\text{taking logs: } 0 = N \log 1.001 + \log B$$

Simultaneously, the number $-N \log_{10} 1.001$ is calculated in register A , by subtracting the log constant, .00043402 ($= \log 1.001$) from it once for each cycle performed.

Therefore:

$$A \text{ (final value of register A)} \approx -N \log_{10} 1.001$$

$$\text{substituting for } N \log 1.001 \text{ from above : } A \approx \log_{10} B$$

Signs and exponents are not affected by this operation. Register C counts the number of cycles performed. This used as a safety measure to ensure that the operation will stop after 10000 cycles if an attempt is made to find the log of zero.

13. **Exp.** This operation is used to calculate antilogs. The operation starts with the number whose antilog is to be found in register A, and 1.0 in register B. The process is exactly the same as the log process, except that the log constant is *added* to register A, and the signal B/1000 *subtracted* from register B each cycle. The iteration continues until there is a carry into the 9th decade of register A.

This is equivalent to the calculation:

$$N = \frac{-A}{\log(1.001)}$$

$$B = 1.0 \times (.999)^N$$

$$\text{hence: } N \log(1.001) = -A$$

$$N \log_{10} .999 \approx A$$

$$\text{since } \log 1.001 \approx -\log .999$$

$$\text{taking antilogs: } (.999)^N \approx 10^A$$

$$B \approx 10^A$$

(i.e. antilog A)

where A = initial value of register A

B = final value of register B

N = number of cycles performed

Signs, exponents and the contents of register C are not affected by this operation. It cannot continue for longer than 1/.00043402 (= 2305) cycles, regardless of the initial contents of the registers.

14. **Polar.** In a cycle of the "polar" operation, the B/1000 signal is added to register A, and the A/1000 signal subtracted from register B. The operation continues until a borrow from the 9th decade of B occurs (i.e. register B becomes negative). The number of cycles performed is counted by the iteration counter (register C). At the beginning of this operation, register A contains the "in-phase" component of the result of the measurement, register B the "quadrature" component, and the iteration counter contains zero. Each cycle is equivalent to rotating the vector represented by A and B towards the real axis by an angle of .001 Radians. This continues until the "quadrature" component becomes zero. At this point, the real part of the vector (the contents of register A) is equal to its amplitude, R, and the angle through which it has been rotated (i.e. the contents of the iteration counter) is equal to its phase angle, θ . Signs and exponents are not affected by this operation.

As for "Log", the operation will be terminated by the iteration counter after 10000 cycles if an attempt is made to convert a zero vector to polar form. The maximum number of cycles which can legitimately occur (corresponding to a rotation of 90°) is $1000\pi/2$ (= 1571).

15. **Cartesian.** This operation is the reverse of "polar". Cycles are the same as cycles of the polar operation except that the B/1000 signal is *subtracted* from register A, the A/1000 signal is *added* to register B, the iteration counter counts *down* one for each cycle, and iterations continue until the iteration counter reaches zero. The operation starts with the vector amplitude (R) in register A, zero in register B, and the phase angle (θ), in milliradians, in the iteration counter. The operation consists of rotating the vector away from the real axis, in 1 milliradian steps, through an angle θ . Registers A and B are then equal to the "in-phase" and "quadrature" components of the vector.

A borrow occurring in register A will also terminate the "Cartesian" operation. This is a safety measure, as if register A became negative it would be in complement form, which could cause large errors in register B if the process were allowed to continue. The characteristics of this process are such that register A can become negative slightly before the vector has been rotated through 90° (the maximum allowed). Signs and exponents are not affected by this operation.

16. **XDivide, YDivide.** These operations are used in the division routine. In the XDivide operation, the contents of register A are subtracted from the contents of register B repeatedly until register B become negative. The number of cycles performed is counted in the addressed decade of the iteration counter. The division routine is arranged so that the contents of register B are always less than 10 times the contents of register A before the XDivide operation. The maximum number of iterations performed is thus 10. The YDivide operation is exactly the same, except that register A is added to register B until it becomes *positive*, and the iteration counter counts *down* instead of up.

Signs and exponents are not affected by these operations.

For a more complete description of the division routine, see "THE 1170 SOFTWARE".

17. **Decsh.** Within each of registers A and B, it is possible to perform a circular shift of the digits, so that the contents of the registers are divided by ten. Since this circular shift operation would result in the least significant digit of the old register contents becoming the most significant digit of the new contents, this digit is gated out so that it is always zero after a Decsh operation. This is accomplished internally by the registers when commanded to operate in DECSH mode. Signs are not affected by the operation, and the exponents are both increased by one, to keep the magnitudes of the numbers being represented by the registers constant.

18. **Integrate.** In a single cycle of the integrate operation, the least significant digit (the "1" digit) of the "sine" signal, from the sin/cos generator, is added to or subtracted from the least significant digit of register A, and the least significant digit of the "cosine" signal added to or subtracted from the least significant digit of register B. Then (within the same cycle) the source of the input data is changed to the most significant digits (the "10" digits) of the "sine" and "cosine" signals, and these are added to or subtracted from the next digit in the registers (digit no. 6). Carries or borrows into the remaining 7 digits of the registers can occur, but no data is added.

Exponents are not affected by the "integrate" operation, but the signs follow the signs of the registers. These may change many times during a complete integration.

INTRODUCTION TO BOARD 3 (MAINFRAME)

The circuitry housed on board 3 can conveniently be divided into 4 sections as follows:

SIN/COS GENERATOR
DIVIDE BY 10/51 COUNTER
SET 0^0 LOGIC
CHOP SIGNAL GENERATOR

These sections are used only during the integration section of each measurement sequence.

SIN/COS GENERATOR

This section receives a clock (SIN/COS CLOCK) from the divide by 10/51 counter. This clock has 200 pulses per correlator cycle. In response, the sin/cos generator produces two signed 2 digit BCD numbers representing $\sin 2\pi ft$ and $\cos 2\pi ft$, which are fed to arithmetic registers A and B respectively (boards 5 & 6).

DIVIDE BY 10/51 COUNTER

The divide by 10/51 counter has as its input the generator clock and produces as its output the sin/cos clock.

At frequencies below 1kHz, the correlator and generator run at the same frequency, f . The generator clock ($2000f$) is divided by 10 to produce the sin/cos clock at frequency $200f$.

At frequencies greater than or equal to 1kHz but below 10kHz the correlator operates in a heterodyning mode at $1/51$ the operating frequency f . The generator clock ($200f$) is divided by 51 to provide the sin/cos clock. A further divide-by-4 counter produces the heterodyning signal at a frequency of $50f/51$.

At frequencies of 10kHz and above the correlator again operates in a heterodyning mode but at a fixed frequency of 1kHz. A fixed frequency of 2MHz is divided by 10 to produce 200kHz for the correlator sin/cos clock.

The sin/cos clock is wire-OR-able, enabling the correlator frequency to be modified. This is used in particular by the 1185 Harmonic Analysis option, which adds clock pulses to the sin/cos clock, causing the correlator to run at a multiple of its fundamental frequency.

The basic sin/cos clock (before wire-OR-ing) is fed to the n -cycle counter (renamed N-CYCLE CLOCK), so that integration is always for a whole number of cycles of the correlator *fundamental* frequency.

SET 0^0 LOGIC

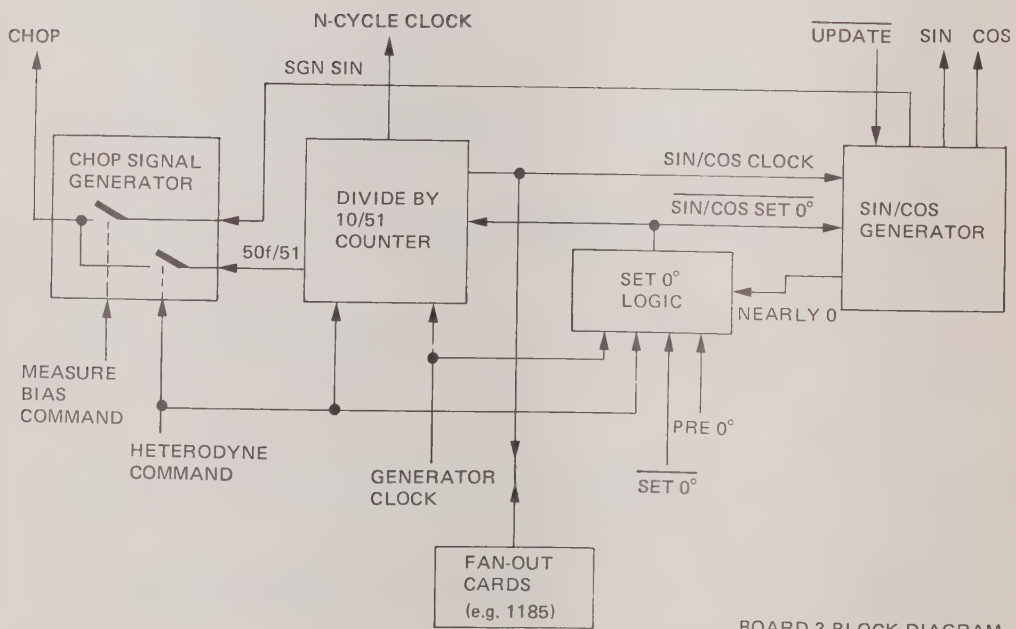
The correlator must be set to 0^0 whenever one of the following two cases apply.

- (a) when the generator passes through 0^0 (or $\geq 1\text{kHz}$, every 51 times the generator passes through 0^0) and,
- (b) when the external world sets the generator to 0^0 .

Case (a) is indicated by the $\text{PRE } 0^\circ$ signal and case (b) by the $\overline{\text{SET } 0^\circ}$ signal. The $\text{SET } 0^\circ$ logic combines these two signals, disables 50 out of 51 0° pulses if $f \geq 1\text{kHz}$, and produces a signal ($\text{SIN/COS SET } 0^\circ$) to set the sin/cos generator and the divide by 10/51 counter to the 0° state.

CHOP SIGNAL GENERATOR

The input system requires a square wave signal (CHOP) by which to multiply the input signal when between 1kHz and 9.999kHz. When the machine is heterodyning the 50f/51 CHOP signal is used, and when measuring bias the correlator polarity signal (SGN SIN) is used.



BOARD 3 BLOCK DIAGRAM

INTRODUCTION TO BOARD 8 (MAINFRAME)

Board 8 houses "Register C", also known as the "iteration counter" or "timer counter". Its function is to count the cycles performed in an iterative operation (LOG, POLAR, CARTES, or a step in the division routine, XDIVIDE, YDIVIDE), and to measure the time taken by the integration operation.

It consists of the following functional blocks:-

COUNTER

This is a 6 digit, synchronous, up/down counter (IC7 to 12, plus associated gates). The mode of the counter (UP or DOWN) is controlled by a wire from the Decode logic (board 7). The counter is arranged so that the clock may be applied to any of its 6 digits, thus altering the "significance" of the clock. This is controlled by the three decade wires.

DECADE No.	CLOCK SIGNIFICANCE
0	100,000 bits
1	10,000 bits
2	1,000 bits
3	100 bits
4	10 bits
5	1 bit
6 or 7	0 (no count)

Digits less significant than the addressed digit are not affected by the clock. Carries or borrows into digits more significant than the addressed digit occur normally.

Example Decade No. = 3
 UP/DOWN = UP

Initial contents	005741
After 1 clock pulse	005841
2	005941
3	006041
4	006141
	etc.

Any one of the 6 digits of the counter may be loaded from the data bus. If the LOAD C wire (from Decode logic) is high, a pulse on the ITERATION CLOCK wire, which occurs once for each cycle performed by the arithmetic unit, will cause the digit on the data bus to replace the addressed digit in the counter. The old digit is lost. Unaddressed digits are not affected by a load operation. If the decade number is 6 or 7, none of the digits are affected. A CLoad operation (see Decode logic truth table) consists of a "read" cycle, which does not affect the contents of registers A or B, performed with the LOAD C wire high.

DATA OUTPUT MULTIPLEXER

Any one of the 6 digits of the counter may be read onto the data bus. The multiplexer section receives the data from each of the 6 digits, selects the output from the addressed digit (if the decade number is between 0 and 5) and reads it onto the data bus if the ENABLE C line (from the control logic) is high. The multiplexer section consists of 6 sets of 4 gates (IC1 to 6) which are wire-OR-ed together, a set of "enable" gates (IC22) and a set of 4 drivers for the data bus (IC24).

CLOCK CONTROL

This section consists of IC27a and IC25c.

During single cycle operations, the iteration counter is not affected. In this case the ITERATE wire and the INTEGRATE wire (from Decode logic) are both low, and the counter receives no clock.

During iterative operations, the counter is required to count the number of cycles performed. In this case the ITERATIVE wire is high, and the counter counts the number of pulses on the ITERATION CLOCK wire, which is equal to the number of cycles performed by the arithmetic unit.

During integration, the counter is required to measure the time of integration. The INT wire is high, and the ITERATE and the BUSY wires low. The counter thus counts TIMER CLOCK signal (see "CONTROL OF INTEGRATION").

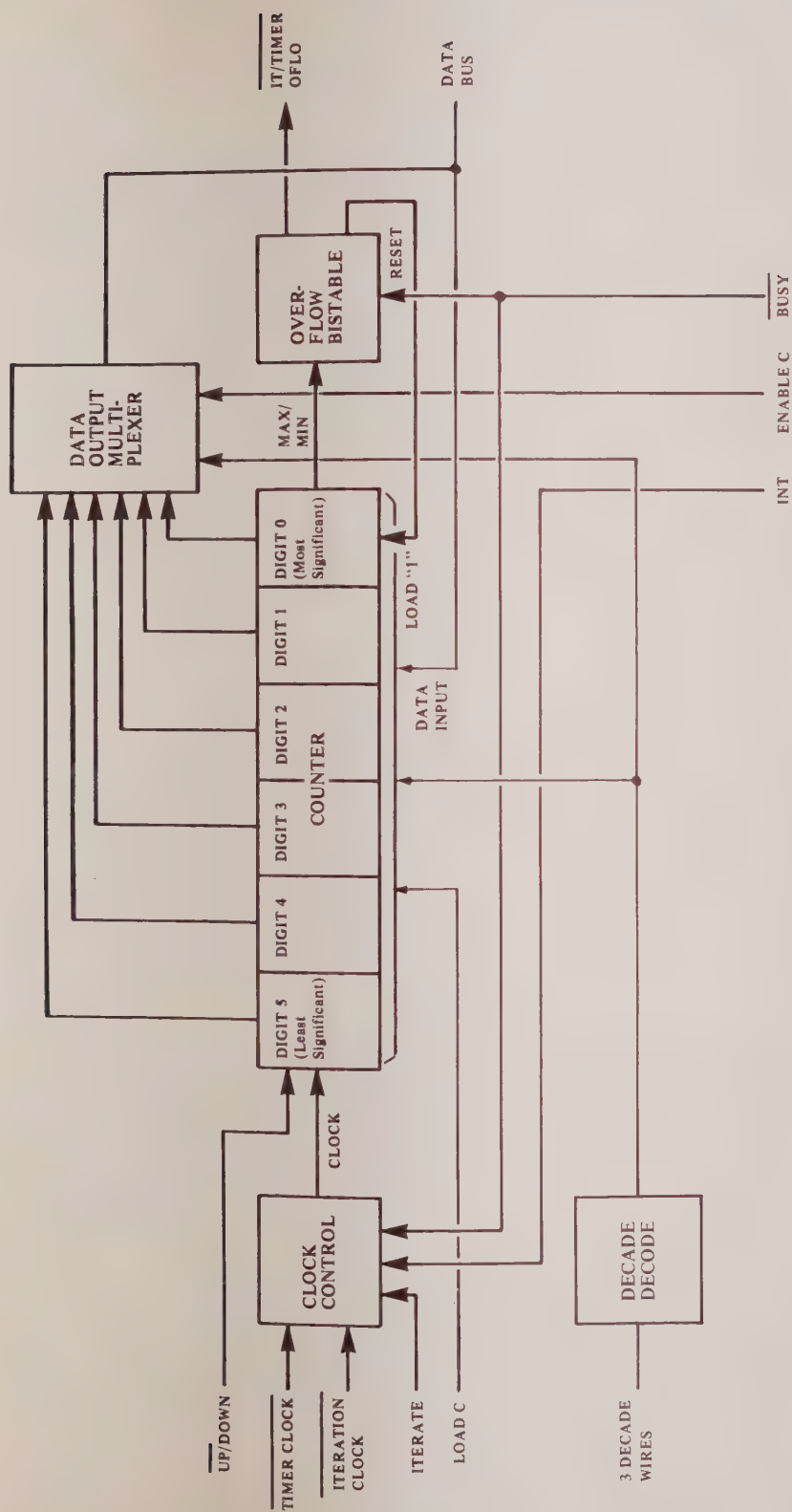
OVERFLOW BISTABLE

This section produces an output (TIMER/ITERATION OVERFLOW) to the sequence logic whenever the part of the counter which is selected counts to zero, either by overflowing (when counting UP) or by counting DOWN to zero. This is used, during iterative operations, to terminate the operation, or, during integration, to initiate an INT.DECSH operation (see "CONTROL OF INTEGRATION"). The signal is derived from the MAX/MIN output from the most significant digit of the counter.

The signal is derived from the MAX/MIN output from the most significant digit of the counter. This is used directly when the counter is counting DOWN (the state zero is the MIN state, i.e. the state immediately before overflow) but is delayed by one clock pulse by a bistable (IC28) when counting UP, as the state zero is reached one pulse *after* the MAX state (i.e. it is the state immediately *after* overflow). The bistable is reset by the BUSY signal at the beginning of every operation.

This section consists of IC28, IC27b, IC20d and e, IC25d and IC23c. Logic is provided so that, during integration (when the INT wire is high), an overflow causes a "one" to be loaded into the most significant digit of the counter. Whenever INT is high, the number "one" is placed on the data inputs of IC12 (this is accomplished by IC18c and IC21b, c and d). When an overflow occurs, a pulse appears on the LOAD input of IC12 (pin 11), causing "one" to be loaded, (accomplished by IC19b). During integration, the counter goes through the states:-

999998
999999
100000
100001
100002
etc.



BOARD 8 BLOCK DIAGRAM
(for more detail refer to circuit diagram)

EXPONENT COUNTER

The exponent counter is situated on board 7. It consists of two 4-bit up/down counters (IC10 and IC11), which are used to keep track of the exponents of the contents of registers A and B during shift operations etc. They are known as "Exp A" and "Exp B" respectively. Each of them may be read onto or loaded from the data bus. Two explicit arithmetic unit operations are provided to decrease the contents of either Exp A or Exp B by one ("AExp dec" and "BExp dec"). The operations ATen and BTen also cause the contents of Exp A and Exp B respectively to be decreased by one, in addition to shifting the contents of registers A and B. The operation DTen causes the contents of both Exp A and Exp B to be increased by one, in addition to shifting the contents of registers A and B. If an attempt is made to increment an exponent counter from state 15, it will overflow, and the subsequent state will be zero. The carry out of the counter is lost. Similarly, when counting down, the counters will underflow from zero to 15, and the borrow out of the counter will be lost.

The magnitude of Exp A-Exp B is calculated by a 4-bit adder (IC9) and a set of inverters (IC13) and can be read onto the data bus as Exp C. It cannot of course be loaded explicitly. The sign of Exp C, and a signal which detects that Exp C = 0 (i.e. Exp A = Exp B), can be sensed, via the condition multiplexer, by the control logic. When Exp C is negative (i.e. Exp A > Exp B) it is expressed in 2's complement form.

DETAIL

Loading

If STROBE A and LOAD are high, and the decade number is 7, a pulse on the ITERATION CLOCK wire (which occurs once for every cycle performed by the arithmetic unit) will cause a pulse to appear on the "load" input of IC11 (pin 11) and the digit present on the data bus will replace the current content of Exp A. The old contents are lost (loading of exponent counters is *destructive*). Since an ALoad operation with decade 7 selected will have no effect on register A, Exp A may be loaded exactly as if it were a digit of register A, which is allocated decade number 7.

Loading of Exp B is an exactly analogous process.

Reading

The exponent counters are read onto the data bus via two Quad 2 to 1 line multiplexers (IC8 and IC15). One of Exp A (IC11), Exp B (IC10) or Exp C (IC9) is selected according to the state of the Enable wires (only one of which may be high at a time). It is only read onto the data bus if the decade number is 7. The exponent counters can thus be read exactly as if they were digits in the registers which are allocated decade number 7. It is not necessary to perform a "read cycle", but the control logic does so for the sake of uniformity, and to initiate a data transfer to the store via the store-arithmetic unit data interface.

Counting

The DECSH CMD wire is used as the up/down control wire for both counters. The ITERATION CLOCK signal is used as the clock - the counters are thus incremented or decremented by one for each cycle performed in which they are enabled. Exp A is enabled (by IC20c) if either the ATEN or DECSH CMD wires are high, and Exp B is enabled (by IC20d) if either the BTEN or DECSH CMD wires are high.

Condition Outputs

The sign of Exp C is simply the "carry" output of the adder which computes Exp C. This is the signal EXP C POS. Zero is detected by IC16 a and b and IC17d - this is the signal EXP C ZERO.

DECODE LOGIC

The various parts of the arithmetic unit have a total of 22 control wires, the state of which determines the operation which is performed when the arithmetic unit is commanded to "go". Each of these wires is static throughout an operation - they must be set up before the arithmetic unit receives the $\overline{GO}$ pulse, and must remain set up until the operation is completed (i.e the arithmetic unit removes the $\overline{BUSY}$ signal).

The arithmetic unit can perform 32 different types of operation, each of which is allocated to a particular state of the 5 "instruction code" wires, by which the control logic controls the arithmetic unit, and each of which requires that the 22 control wires are set up to a particular state. The 32 different states of the 5 instructions codes wires are translated into the corresponding 32 states of the 22 control wires by the Decode Logic.

This is situated on board 7, and comprises two 256 bit read only memories, (IC1 and 2), each of which receives the 5 instruction code wires as its address and produces 8 of the 22 control wires. The remaining 6 of the control wires are produced by a one-in-ten decoder (IC3, type 7442) and a number of gates.

The truth table for the Decode Logic, together with the instruction names and the names of the 22 control wires is shown in Table A.

TABLE A DECODE OUTPUTS

[illegible]

Condition Multiplexer

The control logic can sense the state of a total of 32 different wires in the instrument, by means of conditional instructions. The names and meanings of these wires are shown in INTRODUCTION TO THE CONTROL LOGIC, Table B. The sixteen wires in Group 2, which include all those originating within the arithmetic unit, appear on board 7, and are multiplexed to two wires by means of two 8-to-1 line multiplexers. The 8 wires with numbers between 0 and 7 are multiplexed onto the ARITH COND 1 wire by IC5. The 8 wires with numbers between 8 and 15 are multiplexed onto the ARITH COND 2 wire by IC6. Both of these multiplexers are addressed by the least significant three instruction code wires.

Arith Bistables

Two bistables are provided for use by the control logic as memory elements or as a counter. The bistables are arranged as a two-bit "down" counter, and are controlled by the 6th instruction code wire (the "32" bit of the instruction code). The counter is clocked by the BUSY signal only if this wire is high - it is thus clocked one for each arithmetic unit instruction with a code between 32 and 63 (these 32 codes are otherwise exact duplicates of the codes between 0 and 31).

The state of the least significant bistable (which changes state for every operation with a code between 32 and 63) can be sensed as condition 11, and the most significant bistable (which changes state when the least significant bistable changes from 0 to 1) can be sensed as condition 12. No means of resetting the bistable explicitly is provided.

Input System Settling Delay

A monostable (IC7) is provided for use as a delay after changing the input range (during the auto-range sequence) or the input system mode (during a reject bias measurement) to ensure that the input system has recovered from any overload state before commencing a measurement. The monostable is triggered by a pulse output from the control logic (CMD DELAY) and its output can be sensed as a condition 6. Its period is nominally 30mSec.

THE ARITHMETIC REGISTERS

Introduction

Most of the arithmetic performed by the arithmetic unit is accomplished by two registers, Register A and Register B. Each consists of an identical board, numbered 5, occupying positions 5 and 6 respectively in the instrument. They are referred to in this account as "the board" or "the register" (not to be confused with the term "shift register", which refers to a single integrated circuit), and where signal names are given they refer to Register A, with the corresponding name for Register B in brackets, if different.

Each board can store indefinitely a 9 digit BCD number, with sign, and can add or subtract another 9 digit number ("input data") from it. The board works on a "digit by digit" basis. The input data is added to the register contents one digit at a time, starting with the least significant digit. Each digit requires one clock pulse, to perform a complete addition or subtraction thus requires 9 clock pulses. Clock pulses always occur in groups of nine at a rate of 5MHz. Each group corresponds to an arithmetic unit "Cycle". Iterative operations are made up of many additions or subtractions, and thus require many cycles.

Data Timing

The least significant digit of the input data is accepted by the board on the first clock pulse of the cycle, and the most significant digit on the last clock pulse. All sources of input data must be timed accordingly. The least significant digit must be present before and until the first clock pulse (when it is accepted by any board that is using it as input data). It is then replaced by the second digit in readiness for the second clock pulse, and so on, until the ninth (last) clock pulse, when the most significant digit is accepted by the board, and is replaced by the least significant digit in preparation for the next cycle.

Control Wires

The board is controlled by a number of control wires. These can be divided into two groups:

a) Sequential control wires.

These originate on board 4 ("Sequence logic"), and may change pulse by pulse through the cycle. They include the clock signal mentioned above.

b) Static control wires.

Most of these originate on board 7 ("Decode logic"). They do not change during a cycle (or only at points in the cycle where they are not active).

These are detailed in Table 1.

a) Sequential control wires.

1. $\overline{\text{PRECLOCK}}$
2. $\overline{\text{CPO}}$
3. OUTPUT LATCH STROBE
4. MPX STROBE
5. MPX ADDR 1

b) Static control wires.

REGISTER A	REGISTER B (if different)
1. SGN V	
2. SGN (SIN)	SGN (COS)
3. ADD A CMD	ADD B CMD
4. ADD B CMD	ADD A CMD
5. POS B	POS A

6.	INH. SGN CH.	
7.	LOAD	
8.	DECSH	
9.	DEC 6	
10.	CLEAR	
11.	DEC 6. DEC 7	
12.	MPX ADDR 2	
13.	MPX ADDR 4A	MPX ADDR 4B
14.	STROBE A	STROBE B
15.	INT.	

TABLE 1

Data Communication

Data is communicated to and from the iteration counter or the store, one digit at a time, via the arithmetic unit data bus. This is a two directional, negative logic, four wire, data bus. Each register is provided with an "enable" wire. When the enable wire for a register is high, a previously selected digit is read from the register onto the bus, where it will remain until it has been accepted by the receiving device (this may take up to 512μ Sec. for the store). When the enable wire is low, a zero is read onto the bus (i.e. four logic highs, as the bus operates in negative logic), freeing the bus for use by other registers. The digit which is read onto the bus is selected by means of the three "Decade" wires.

Internal Organisation

With the single exception of the data output latch, the board is composed entirely of synchronous logic. All bistables and shift registers are driven by the same clock signal, which is derived by a single inverter from the PRECLOCK signal. The heart of the board is a loop consisting of four 8 bit shift registers, a set of four bistables, and a BCD processor section (See Fig. 1.). The processor is divided into two parts, each consisting of combinational logic only, which are separated by the set of bistables. The four shift registers operate in parallel, so that data is shifted out of them into the processor section four bits (one BCD digit) at a time. Each digit passes through the shift registers, through the first part of the processor and into the set of bistables, then through the second part of processor and back into the shift registers. There are nine stages in this loop, so that at the end of a group of nine clock pulses, each digit has returned to its "home" position, having passed through all nine stages, and through the processor.

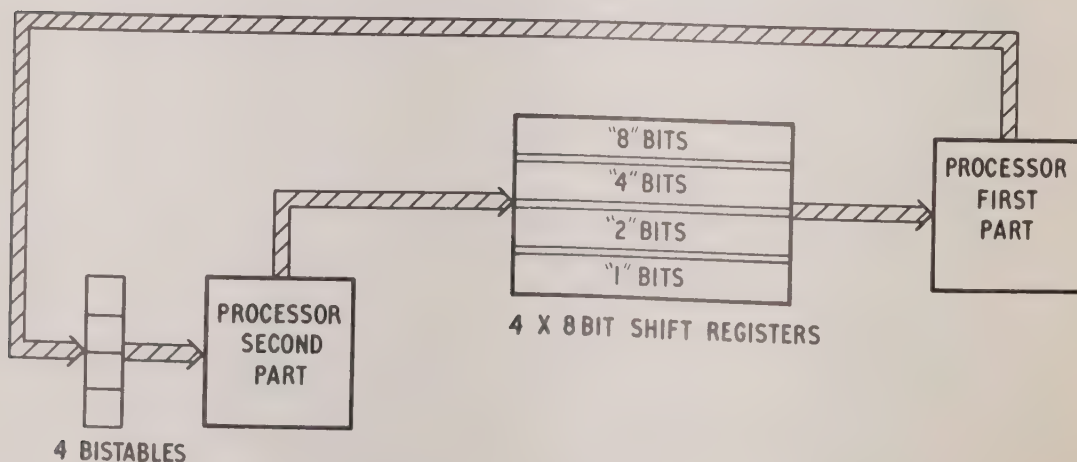


Fig. 1 Arithmetic Register Central Loop.

Processor (See Fig.2)

The first part of the processor performs a binary addition or subtraction of a digit of the data from the corresponding digit of the register contents, and computes the resulting decimal carry or borrow bit. Subtractions are performed by forming the ones complement of the input data (performed by a set of exclusive - OR gates) before it is added to the register contents. The intermediate result formed by the first part of the processor enters the set of bistables where it is stored until the next clock pulse. An "abnormal carry" bistable (ABN CARRY) stores the carry information and an ADD' bistable stores the add/subtract mode until the next clock pulse. A "carry/borrow" bit is computed from the outputs of these two bistables for addition to the next digit processed. No carry or borrow into the least significant digit is allowed - the "carry/borrow" bit is forced to the state marked "normal" when this digit is being processed (see table 2).

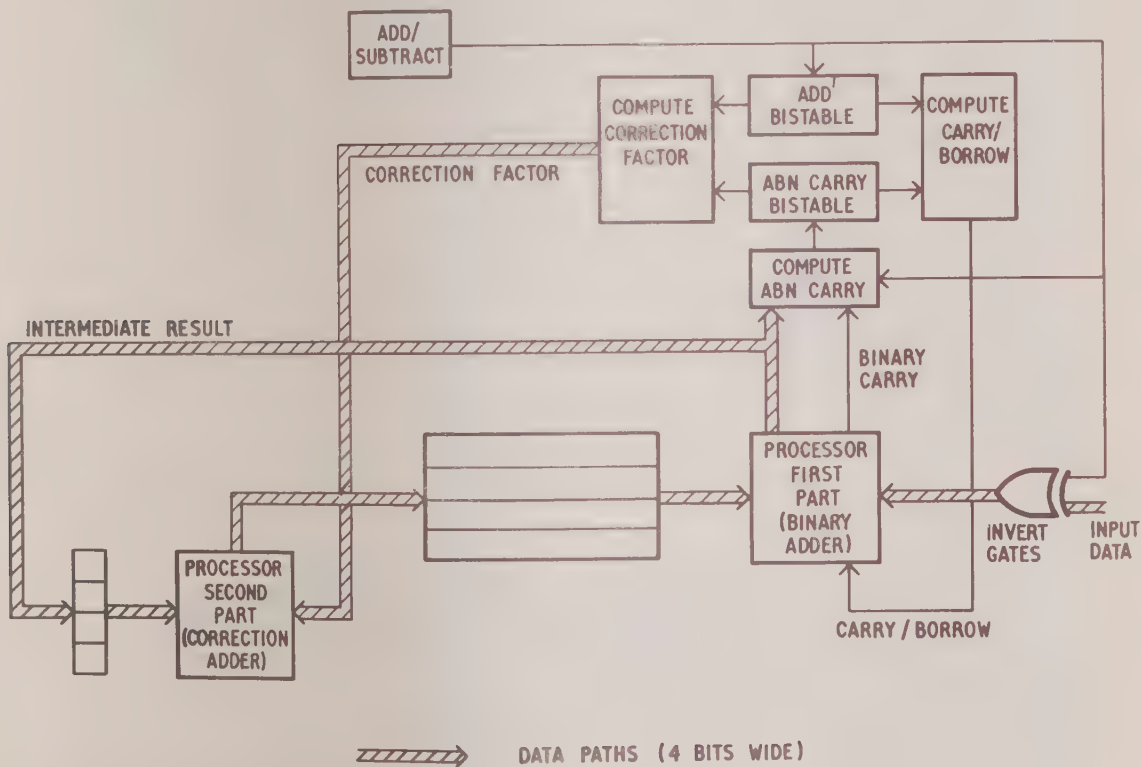


Fig. 2 Processor.

			CARRY/BORROW	MEANING	ABN CARRY	CORRECTION FACTOR
ADD	sum < 10	0	0	normal	0	0
	sum ≥ 10	1	1	carry one	1	6
SUBTRACT	difference < 0	0	0	borrow one	1	10
	difference ≥ 0	1	1	normal	0	0

TABLE 2

The second part of the processor is a "correction adder". It adds a correction factor computed from the output of the ABN CARRY and ADD bistables to the intermediate result, to give the final result. The "16" bit of this result is ignored, and it is then a true BCD digit (see table 3).

COLUMN	ADD					SUBTRACT					
	1	2	3	4	5	6	7	8	9	10	11
0	0	0	0	0	0	- 10	6	0	10	16	0)
1	0	0	0	1	1	- 9	7	0	10	17	1)
2	0	0	0	2	2	- 8	8	0	10	18	2)
3	0	0	0	3	3	- 7	9	0	10	19	3)
4	0	0	0	4	4	- 6	10	0	10	20	4)
5	0	0	0	5	5	- 5	11	0	10	21	5) borrow
6	0	0	0	6	6	- 4	12	0	10	22	6)
7	0	0	0	7	7	- 3	13	0	10	23	7)
8	0	0	0	8	8	- 2	14	0	10	24	8)
9	0	0	0	9	9	- 1	15	0	10	25	9)
10	1	6	16	0	)	0	16	1	0	16	0
11	1	6	17	1	)	1	17	1	0	17	1
12	1	6	18	2	)	2	18	1	0	18	2
13	1	6	19	3	)	3	19	1	0	19	3
14	1	6	20	4	)	4	20	1	0	20	4
15	1	6	21	5	) carry	5	21	1	0	21	5
16	1	6	22	6	)	6	22	1	0	22	6
17	1	6	23	7	)	7	23	1	0	23	7
18	1	6	24	8	)	8	24	1	0	24	8
19	1	6	25	9	)	9	25	1	0	25	9

TABLE 3

COLUMN

- 1 Input data and carry bit added to register contents.
Equal to intermediate result (output of processor first part).
- 2 New CARRY/BORROW bit ("1" = carry).
- 3 Correction factor.
- 4 Sum of intermediate result and correction factor
- 5 Final result (ignoring "16" bit).
- 6 Input data and borrow bit subtracted from register contents.
- 7 Intermediate result (output of processor first part).
- 8 New CARRY/BORROW bit ("0" = borrow).
- 9 Correction factor.
- 10 Sum of intermediate result and correction factor.
- 11 Final result (ignoring "16" bit).

Data Outputs

Three outputs are provided from each board for use as input data. Since digits are processed one at a time, each having ten times the significance of the previous digit, the significance of a data output can be determined by choosing the timing of the digit relative to the clock. Normally the least significant digit is produced in time to be accepted as input data on the first clock pulse of a cycle and so on. In this case the data output has a significance of "1". If the output is taken from a point one

stage later in the shift register, the data will be delayed by one clock pulse (i.e. the least significant digit is produced in time to be accepted on the second clock pulse of a cycle, etc.) and will have a significance of "10". If the digits are advanced by taking from a point earlier on the shift register, the significance of the data is reduced by ten times for each clock pulse advance. The three data outputs provided have significances of "10", "1" and "1/1000".

Input Multiplexer

Each board can select one of 8 sources from which to take its input data. This is performed by a set of four 8-to-1 line multiplexers. The multiplexers have a 3 bit address. The '1' and '2' bits are common to the two boards - separate "4" bits are provided, to allow a certain amount of flexibility in the selection of data sources. The "2" and "4" bits of the multiplexer address are static control wires - the "1" bit is a sequential control wire, although it is only used as such during the "integrate" operation, when its function is to switch the input data source from the "1" digit of the SIN and COS signals to the "10" digit, after the first clock pulse of the cycle. For the allocation of multiplexer addresses, see table 4.

Mpx Address	Register A	Register B
0	SIN 1	COS 1
1	SIN $\overline{10}$	COS $\overline{10}$
2	10A	10B
3	DATA BUS	DATA BUS
4	LOG. CONST.	B/1000
5	B/1000	A/1000
6	A	B
7	B	A

TABLE 4

Note: The multiplexer address shown here refers to the signals appearing on boards 5 and 6. It should be noted that the "1" bit of the MPX ADDRESS is inverted with respect to the MPX 1 CMD wire originating on board 7.

Strobe Gates

A set of gates is provided to enable none, some, or all of the nine digits of the input data to be added. The "pattern" of digits added to the register is determined by the MPX STROBE wire, a sequential control wire common to both boards. Separate static control wires (STROBE A and STROBE B) are provided, allowing neither, either or both registers to accept input data. When the input data is disabled, zero is added to or subtracted from the register contents, and the multiplexer address is of course irrelevant.

Clear Gates

A set of gates is provided which allows the register contents to be discarded before entering the processor section of the board. These are controlled by the CLEAR wire, a static control wire common to both boards. If this wire is low, the input data is added to or subtracted from zero. This enables the register contents to be cleared or inverted.

Decsh Gates

A set of four AND-OR-INVERT gates is provided so that the data in the register can be made to bypass the processor and the set of four bistables. This means that each digit requires only 8 clock pulses to reach its "home" position. Thus at the end of the cycle each digit has reached one position further, its weight being reduced by a factor of ten. This has the overall effect of shifting the contents of the register down one digit position, dividing its magnitude by ten. The AND-OR-INVERT gates are controlled by the DECSH wire, a static control wire common to both boards. Logic is provided to ensure that the most significant (9th) digit is equal to zero after a Decsh operation (during an integration operation - i.e. while the INT wire is high - the most significant digit will be made equal to 9 after a Decsh operation, if the register contents are negative, as they will be in 10's complement form).

Add Gates

Normally the add/subtract mode of the board is controlled directly by the ADD A CMD (ADD B CMD) wire. However, if both ADD A CMD and ADD B CMD are low, the add/subtract mode is controlled by the sign of the register contents, such that the board will only subtract if the contents are negative. This feature is provided for use by the Complement operation (the only operation for which both ADD A CMD and ADD B CMD are low).

During Integration (i.e. while the INT wire is high) the add/subtract mode is controlled by the SGN SIN (SGN COS) and SGN V wires. An exclusive - OR gate forms the product of these two signals, which then determines the add/subtract mode for the cycle to be performed.

Sign Bistable

Each board is provided with a sign bistable to keep track of the sign of the register contents during add and subtract (and integrate) operations. In order for the bistable to operate correctly, it is necessary for the register contents to be in 10's complement form if negative. The bistable works on the principle that an examination of the sign of the register contents, and whether they are being added or subtracted, will determine whether an operation will change the contents in a direction towards zero or away from it. If the contents will change in a direction away from zero, or if the board is not adding or subtracting, a sign change is impossible, and any change of state of the bistable is inhibited. If the contents of the register will change in a direction towards zero, the new sign can be determined from the ABN CARRY signal (see table 5). Due to propagation delay considerations, the new sign must be computed by a complex set of gates from the data outputs of the first part of the processor, rather than from the ABN CARRY signal. A static control wire which will inhibit changes of the sign bistables regardless of other conditions, is provided (INH, SGN, CH.).

SIGN OF REGISTER CONTENTS	SIGN OF INPUT DATA	ADD/SUBTRACT MODE	SIGN CAN CHANGE	ABN CARRY	NEW SIGN
+	+	ADD	NO	(0	-
+	+	SUBTRACT	YES	(1	+
+	-	SUBTRACT	NO	(0	-
+	-	ADD	YES	(1	+
-	-	ADD	NO	(0	-
-	-	SUBTRACT	YES	(1	+
-	+	SUBTRACT	NO	(0	-
-	+	ADD	YES	(1	+

TABLE 5

It is assumed that input data in an addition or subtraction operation is coming from the other register. The signal POS B (POS A) indicates whether it is positive or negative. During integration (i.e. when the INT wire is high), this signal is disabled, as the value of SIN (COS) is always regarded as positive (negative values are obtained by subtracting the positive value).

The sign bistables may be loaded from the "1" bit of the data bus if the LOAD, DEC 6 and STROBE A (STROBE B) wires are high, and the $\overline{\text{INH. SGN. CH.}}$ wire is low.

Output Latch

A four bit latch is provided to enable any one of digits 0 to 5 to be latched during a cycle for subsequent reading onto the data bus. It is supplied with a strobe pulse (OUTPUT LATCH STROBE), whose position in the cycle is determined by the DECADE wires, from board 4. The contents of the latch are read onto the data bus if the $\overline{\text{ENABLE A}}$ (ENABLE B) and DEC 6 $\overline{\text{DEC 7}}$ wires are high. The contents of the sign bistable are read onto the "1" bit of the data bus if the ENABLE A (ENABLE B) and DEC 6 wires are high - they are also available as a separate signal, POS A (POS B), for use by the control logic (via the condition multiplexer).

Dec 9 Zero Gate

An output signal $\overline{\text{DEC 9 A ZERO}}$ ($\overline{\text{DEC 9 B ZERO}}$) is provided to indicate to the control logic (via the condition multiplexer) whether the 9th digit of the register contents is zero.

Delay Bistables

All signals present on the edge - connector of the board are timed so that events associated with the least significant digit occur on the first clock pulse of the cycle, and so on. Static control signals, which affect all 9 digits, change between cycles. However, they may affect various different points on the central loop of the register. The least significant digit may not reach the point affected (the "control point") until one or two clock pulses after the beginning of the cycle, and the most significant digit may not reach it until one or two clock pulses after the beginning of the succeeding cycle, which may not occur for some time after the cycle in question. Bistables are necessary to delay the arrival of control signals until the least significant digit of the register contents arrives at the control point, and to store the signals until the most significant digit has passed this point on the loop.

Bistables in this category are:

- | | |
|----------------------------------|--------------------------|
| 1) Set of 4 input data bistables | (one clock pulse delay) |
| 2) ADD bistable | (one clock pulse delay) |
| 3) ADD' bistable | (two clock pulses delay) |
| 4) INH. SGN. CH bistable | (one clock pulse delay) |
| 5) CLEAR bistable | (one clock pulse delay) |
| 6) DECSH bistable | (two clock pulses delay) |

Some control signals, while they are static in the sense that their effect is constant for all 9 digits, are not maintained for the whole of the cycle. Bistables which store these signals must not be allowed to change state until the end of the cycle, if the input signal should change. This is achieved by routing the outputs of these bistables back to their inputs for all clock pulses when they are not permitted to change state. The bistables to which this applies are:

- 1) ADD bistable
- 2) DECSH bistable
- 3) POS A (POS B) bistable (slightly different, in that it is the ABN CARRY information that is not maintained, rather than the control signals)

The signal $\overline{\text{CPO}}$ is provided to indicate the first clock pulse of the cycle. A signal indicating the second pulse is generated on the board (CPO'). These signals are used to control changes of state of the bistables shown above, and also to control sections of the board which require a mode change

at some point in the cycle, e.g.:

- 1) Carry and borrow must be inhibited for the first digit.
- 2) Decsh gates must force the 9th digit to zero or nine.

Logic Convention

All data inputs and outputs to the board are in negative logic. However, some parts of the board (principally the processor and the set of 4 bistables) operate in positive logic. These are indicated in fig. 3.

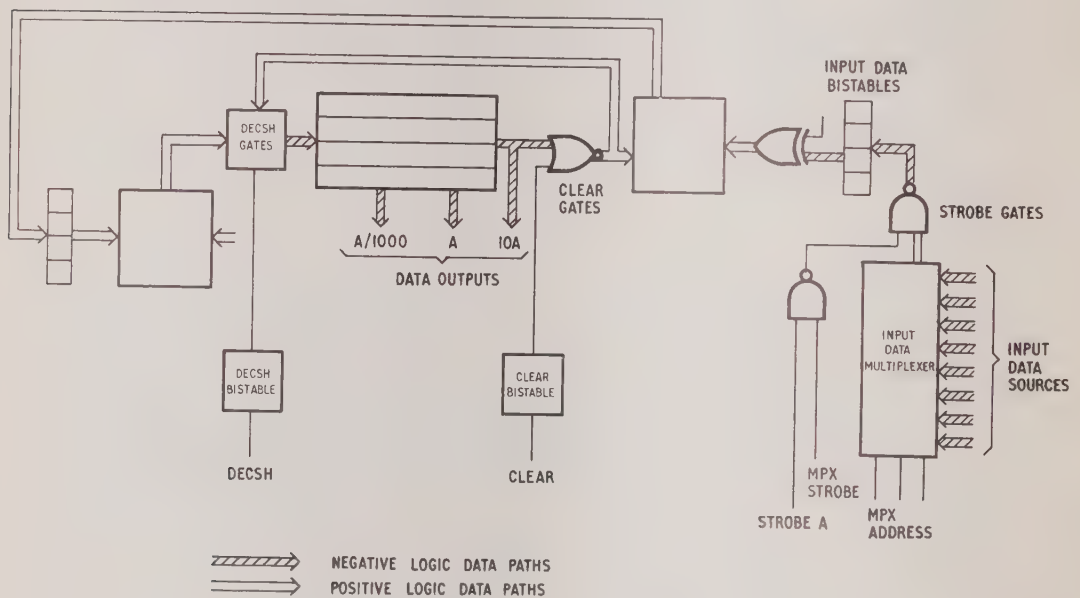


Fig. 3 Logic Data Paths.

INTRODUCTION TO SEQUENCE LOGIC

The "sequence logic" is situated on board 4. Its function is to interlock the arithmetic unit and control logic timing, and to produce all clocks and sequential signals required by the arithmetic unit. The operation of the sequence logic will be described for all operations except for integration, in this chapter.

The sequence logic can be subdivided into the following sections.

1. Clock generator
2. Sequential control signal generator
3. Clock enable logic
4. Sequence control

1. Clock Generator

The clock input to the board is a continuous 10MHz clock. A continuous 5MHz clock is derived from this by a bistable operating as a divide by 2 stage. The 5MHz clock drives most of the bistables in the sequence logic.

The PRECLOCK signal is also generated by this section of the board. This signal is used as a clock by the arithmetic register boards (5 and 6). It is a train of pulses, occurring in groups of 9, at a rate of 5MHz. The pulses within a single arithmetic unit operation are continuous, but the number of pulses is always a multiple of 9. Incomplete cycles are not allowed. An 8 bit shift register is used to ensure that pulses occur in groups of 9. The shift register is clocked by the PRECLOCK signal. Its input (named CPO) is high if any one of its stages is set to "0". If all the 8 stages are set to "1", the input (CPO), which will become the state of the first stage after the next clock pulse, is low. There are thus 9 states through which the shift register can pass:-

STAGE	1	2	3	4	5	6	7	8	Input (<u>CPO</u>)
	1	1	1	1	1	1	1	1	0
	0	1	1	1	1	1	1	1	1
	1	0	1	1	1	1	1	1	1
	1	1	0	1	1	1	1	1	1
	1	1	1	0	1	1	1	1	1
	1	1	1	1	0	1	1	1	1
	1	1	1	1	1	0	1	1	1
	1	1	1	1	1	1	0	1	1
	1	1	1	1	1	1	1	0	1

The PRECLOCK signal is generated by a bistable clocked by the 10MHz clock. The output of this bistable follows the 5MHz clock if either the CPO signal or the CLOCK ENABLE signal is high. If both these signals are low, the output of the PRECLOCK bistables is permanently high (i.e. the clock stops). This means that the clock can only stop with the shift register in the first state shown above, which occurs once every 9 pulses. The number of clock pulses which occur in a group must be a multiple of 9. The CLOCK ENABLE signal is used to initiate or maintain a group of clock pulses. If the signal is removed the clock will stop when the next multiple of 9 is reached. A signal (C in P) indicating that a cycle is in progress, is produced for use by the "sequence control" section.

2. Sequential Control Signal Generator

A number of "sequential control signals" are produced whose state depends upon the stage in the cycle which has been reached. These signals are used by other parts of the arithmetic unit. They are generated from the outputs of the shift register and the position of the "0" in the shift register, if any, indicates which of the 9 clock pulses has been reached.

The signals are :

	SIGNAL	USED BY BOARDS
1.	$\overline{\text{CPO}}$	5,6
2.	ITERATION CLOCK	7,8
3.	MPX STROBE	5,6
4.	OUTPUT LATCH STROBE	5,6
5.	MPX ADDR 1	5,6
6.	LOG CONST. $\overline{8}$	5
7.	LOG CONST. $\overline{4}$	5
8.	LOG CONST. $\overline{2}$	5
9.	LOG CONST. $\overline{1}$	5

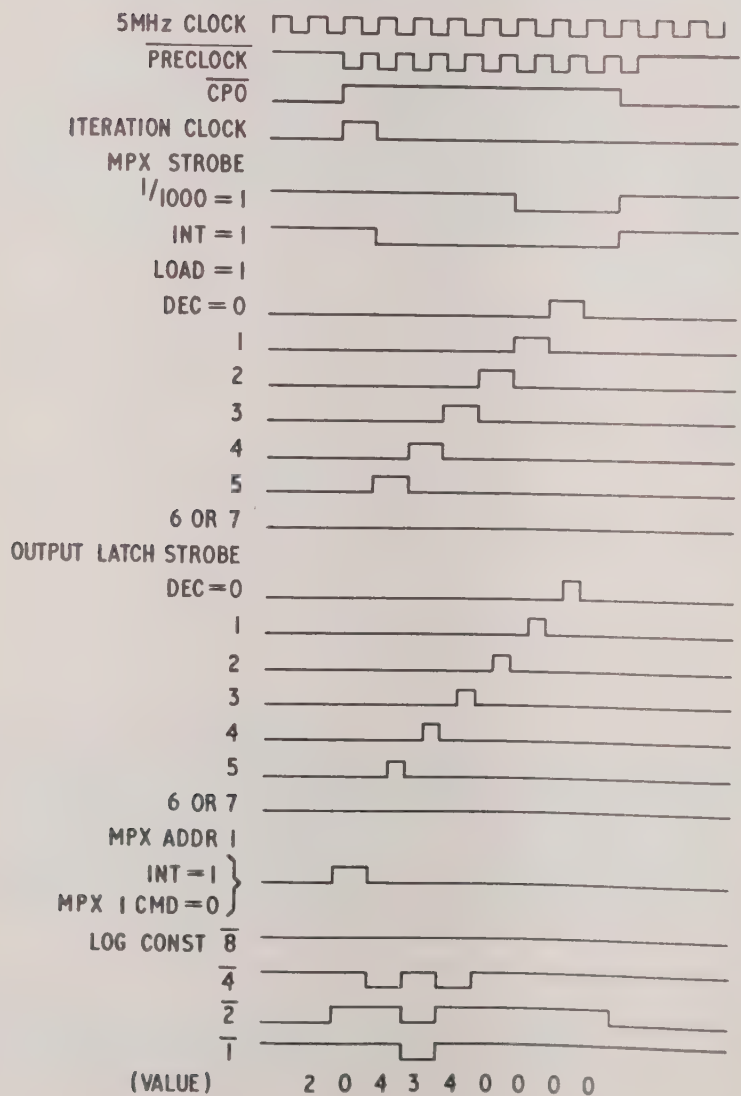


Fig. 1 Arithmetic Unit Timing Diagram.

3. Clock Enable Logic

This section is composed of gates only. Its function is to initiate an arithmetic unit operation, and to terminate it when the appropriate conditions are satisfied. It has a number of modes of operation, which are selected by the STOP CODE A and STOP CODE B wires.

a) Single cycle operations. (See Fig. 2).

STOP CODE A = high

STOP CODE B = high

Nine clock pulses are produced in this mode. The CLOCK ENABLE wire remains high for one clock pulse (200nSec) only to initiate a cycle, and the operation finishes at the end of the cycle.

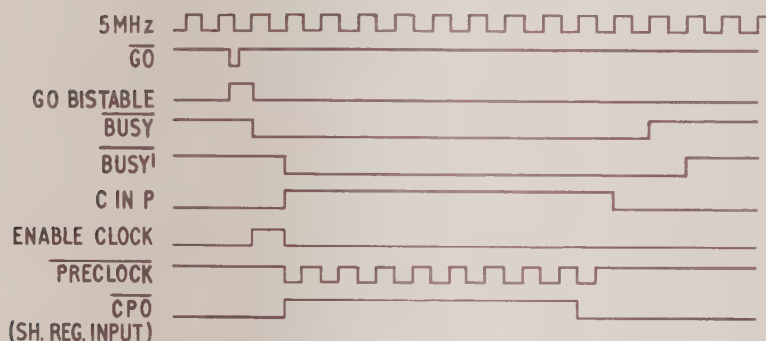


Fig. 2 Single Cycle Operation

b) Iterative operations. (See Fig. 3).

i) STOP CODE A = high

STOP CODE B = low

In this mode cycles continue until either the TIMER/ITERATION OFLO wire goes low or the ABN CARRY A wire goes high. When either of these things happens, the CLOCK ENABLE wire goes low, and the clock stops at the end of the cycle. Since the clock can only finish at one point in the cycle, the state of the ABN CARRY A wire is irrelevant except between the last clock pulse of one cycle and the first clock pulse of the next (the level of this signal may in fact change at any or all clock pulses). Change of state of the TIMER/ITERATION OFLO signal should occur slightly after the 2nd clock pulse of the cycle (i.e. slightly after the iteration clock edge).

If the TIMER/ITERATION OFLO signal is low when an operation is requested, no cycles will be performed. The ABN CARRY signal however is ignored for the first cycle (this signal may have been left high by the previous operation) - if ITERATION/TIMER OFLO is high before the operation, at least one cycle must occur.

ii) STOP CODE A = low

STOP CODE B = high

In this mode the conditions which must be satisfied to terminate the operation are the same as (i) above, except:-

ABN CARRY B is used in place of ABN CARRY A

Both ABN CARRY B and TIMER/ITERATION OFLO are ignored for the first cycle. In this mode, at least one cycle must occur.

In both (i) and (ii) above, the TIMER/ITERATION OFLO signal is assumed to be present if DECADE number 6 or 7 is selected. In this case the operation will stop after no cycles (case (i)) or one cycle (case (ii)) respectively. This is a precaution only, to prevent infinitely long operations when the wrong DECADE is selected.

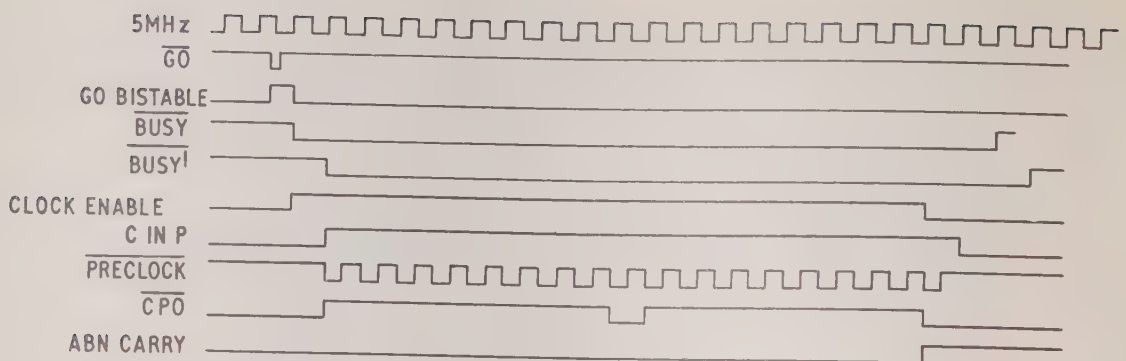


Fig. 3(a) Iterative Operation (Stopped By ABN CARRY).

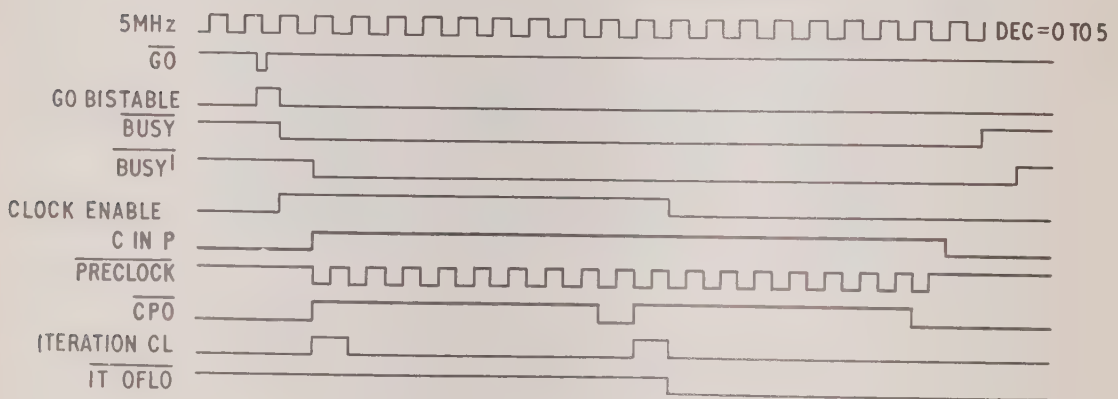


Fig. 3(b) Iterative Operation (Stopped By IT OFLO).

- c) STOP CODE A = low
 STOP CODE B = low
 This mode is never used.

4. Sequence Control

This section consists of a number of bistables and gates. Its function is to accept the command to perform an operation (the $\overline{GO}$ pulse) from the control logic, generate the $\overline{BUSY}$ signal which indicates to the control logic that an arithmetic unit operation is in progress, and to instruct the clock enable logic to initiate the operation.

The $\overline{GO}$ pulse is accepted by an RS bistable and stored until the next 5MHz clock pulse. The $\overline{BUSY}$ bistable is then set (a maximum of 200nS after the leading edge of the $\overline{GO}$ pulse), which causes the $\overline{BUSY}$ signal to the control logic to go low, inhibiting further control logic action. The RS bistable is reset at this point, provided that the $\overline{GO}$ pulse has finished (otherwise it will remain set until $\overline{GO}$ pulse finishes). A $\overline{BUSY'}$ bistable follows the $\overline{BUSY}$ bistable with 1 clock pulse (200nSec) delay. The $\overline{BUSY'}$ signal is used to enable most of the conditions for terminating operations (the $\overline{TIMER/ITERATION}$ OFLO signal is permanently enabled if STOP CODE B = low, causing no cycles to be performed under certain conditions - see 3, b, i above). Initially $\overline{BUSY} = \text{low}$ and $\overline{BUSY'} = \text{low}$. The termination conditions are thus disabled. When $\overline{BUSY}$ goes high, the $\overline{CLOCK ENABLE}$ wire will go high, (except in the special case mentioned in 3, b, i above) and the operation will commence. On the next clock pulse, $\overline{BUSY'}$ will go high, enabling the termination conditions. The operation will continue until these conditions are met.

The BUSY bistable remains set as long as the C in P bistable is set. When the operation is finished, the C in P bistable will reset, and the following clock pulse, the BUSY bistable will reset, allowing the $\overline{\text{BUSY}}$ wire to the control logic to go high. The control logic will then proceed to the next instruction, and the arithmetic unit will remain quiescent until the next $\overline{\text{GO}}$ pulse. The BUSY bistable cannot reset if CLOCK ENABLE is high. This prevents it from resetting at the beginning of an operation, before the C in P bistable is set.

INTRODUCTION TO THE CONTROL LOGIC

The arithmetic unit is only capable of performing simple operations autonomously. Each stage in the calculation of the results or in the calculation of the new frequency in a frequency sweep, involves many such steps. Other parts of the instrument also require commands at various points in the measuring sequence (see Table A). It is the function of the control logic to issue these commands in the correct sequence to perform whatever action is requested by the touch keys. In fact the instrument is performing a continuous sequence of operations whenever it is switched on, as the state of waiting for a command from the front panel involves a sequence of examining in turn each touch key from which a command could come.

Sections requiring commands from control logic.	Nature of commands
1. Arithmetic unit	32 arithmetic operations, including data transfers to and from the store.
2. Store	Read and write commands in conjunction with the arithmetic unit (see above)
3. Keyboard display	Update local display data buffer from the appropriate store location.
4. Keyboard	a. Disable keyboard while the machine is running b. Switch SINGLE button to OFF at the end of the measurement. c. Switch sweep button to OFF at the end of a frequency sweep, or if the synchroniser (1185) is in use.
5. Autorange counter	a. The counter used to control the input range in the autorange sequence is set to the 10mV range at the beginning of the sequence. b. Increment autorange counter.
6. Input system	Various modes may be selected: a. Measure bias b. Reject bias
7. Peripherals	The machine indicates to any peripherals that may be attached (plotter, teletype, computer etc.) that the results are ready to be accepted.

Table A Control Logic Functions

The control logic follows a program of 1024 instructions. Each of these is an 8 bit word, - they are stored in four 2048 bit read-only memory IC's (Board 11, IC's 19, 24, 32, 39). The program includes jump instructions, sub-routines and conditional instructions. An instruction may be internal to the control logic (e.g. a jump instruction, or an instruction setting an internal memory bistable), or may involve one or more other sections of the machine. Conditional instructions are used so that changes in the state of other sections of the instrument may affect the path taken by the control logic through the program. The control logic can monitor the state of various counters and bistables within itself in the same way (see Table B).

ARITHMETIC UNIT CONDITIONS

Group	No.	Name	Source	Meaning
2	0	<u>DEC 9 ZERO A</u>	Register A (Board 5)	Is the 9th decade of register A equal to zero?
2	1	<u>DEC 9 ZERO B</u>	Register B (Board 6)	Is the 9th decade of register B equal to zero?
2	2	EXP C POS	Exponent counter (Board 7)	Is EXP C positive? (i.e. $\text{EXP B} \geq \text{EXP A}$)
2	3	<u>EXP C ZERO</u>	Exponent counter (Board 7)	Is EXP C equal to zero? (i.e. $\text{EXP B} = \text{EXP A}$)
2	4	POS A	Register A (Board 5)	Are the contents of register A positive?
2	5	POS B	Register B (Board 6)	Are the contents of register B positive?
2	11	ARITH BS 1	Board 7	Is bistable no.1 set?
2	12	ARITH BS 2	Board 7	Is bistable no.2 set?

TOUCH KEY CONDITIONS

Group	No.	Name	Source	Meaning
1	4	Measure mode X	Touch keys	Which of keys X, Y, Y/X is selected?
1	5	Measure mode Y	Touch keys	
1	11	Measure sequence SINGLE	Touch keys	Which of keys STOP, SINGLE, RECYCLE is selected?
1	12	Measure sequence RECYCLE	Touch keys	
1	10	Sweep ON	Touch keys	Which of keys OFF, HOLD, UP, DOWN is selected?
1	9	Sweep DOWN/ HOLD	Touch keys	
1	13	Sweep LOG	Touch keys	Which of keys LIN LOG is selected?
1	15	ENTER FREQUENCY	Touch keys	Has the ENTER key been pressed? (with FREQUENCY selected)
1	14	ENTER VOLTS	Touch keys	Has the ENTER key been pressed? (with OUTPUT VOLTS selected)
1	3	REJECT BIAS	Touch keys	Is the REJECT BIAS key selected?

TABLE B

INTERNAL CONDITIONS

Group	No.	Name	Source	Meaning
2	7	INPUT X/ $\overline{Y}$	Input channel bistable	Are the input channel relays set to X or Y?
2	13	$\overline{\text{MEASURE BIAS}}$	Measure bias bistable	Is "measure bias" mode selected?
1	2	MARKER BISTABLE	Marker bistable	Is the bistable set? (local memory element)
1	8	SWEEP BISTABLE	Sweep bistable	Is the bistable set? (i.e. is this the first measurement of a frequency sweep)?
1	6	ARITH DEC 8	Arithmetic decade counter	Is the 8 bit of the counter set?

MISCELLANEOUS EXTERNAL CONDITIONS

Group	No.	Name	Source	Meaning
1	0	INPUT RELAY FLAG	Input relays	Are the relays in the process of changing?
1	1	AUTORANGE OVERLOAD	Autorange logic (Board 17)	Has integration been terminated by an overload during an autorange measurement?
2	10	OVERLOAD	Autorange logic (Board 17)	Has overload occurred during this measurement?
2	14	PERIPHERAL FLAG	Peripherals	Have all peripherals which may be attached to the instrument finished receiving the results, or programming the instrument?
2	9	SYNCHRONISER FLAG	Synchroniser (1185) option	Is the measurement value of the period of the synchronising signal ready for processing?
2	8	$\overline{\text{LEAD/LAG}}$	Lead/lag link (Board 7)	Is the instrument set to measure lead angles (link present) or lag angles (link absent)?
2	6	Input system settling delay	Delay Monostable (Board 7)	Is the delay monostable set? This allows a 30mS period for the input system to settle after altering the range during an autorange sequence.
1	7	STORE OVERLOAD	Store	Is the overload bit set in the currently addressed store word?
2	15	SPARE FLAG		

In order to control the states of other sections of the instrument, various pulse and level outputs are available (see Table D).

PULSE OUTPUT	DESTINATION	FUNCTION
$\overline{\text{GO}}$	Arithmetic unit	Initiate instruction specified by INSTRUCTION CODE lines.
RESET RANGE	Autorange counter	Reset range to 10mV at beginning of autorange sequence.
$\overline{\text{INC. RANGE}}$	Autorange counter	Increment range during autorange sequence.
$\overline{\text{CHANGE FREQ}}$	a) Keyboard display b) Peripherals	Update local display data buffer from frequency or volts location in store. Indicates that results are ready to be output.
$\overline{\text{MOS STORE WRITE}}$	Store	Write current data bus digit into store.
$\overline{\text{RESET OVERLOAD}}$	Autorange logic	Reset overload bistable at beginning of measurement.
$\overline{\text{CMD DELAY}}$	Delay monostable (Board 7)	Initiate input system settling delay (used after changing range in autorange sequence).
RESET SWEEP	Touch keys	Reset sweep buttons to OFF.

LEVEL OUTPUT	DESTINATION	FUNCTION
INSTRUCTION CODE	Arithmetic unit	5 lines - select one of 32 arithmetic unit operations. 1 line - enable programmable arithmetic unit bistables.
DECADE NO.	Arithmetic unit	Select one of 8 decades.
$\overline{\text{MEASURE BIAS}}$	Arithmetic unit Input system	Select "measure bias" mode.
$\text{X}/\overline{\text{Y}}$ RELAYS	Input channel relays	Select channel X or Y
$\overline{\text{COMPUTE}}$	a) RUN lamp b) Peripherals	RUN lamp is on when $\overline{\text{COMPUTE}} = 0$ Control data sourcing and data receiving peripherals.
$\overline{\text{RUN}}$	Touch keys	Disable keyboard while $\overline{\text{RUN}} = 0$ Switch SINGLE button off at end of measurement.
ENABLE $\overline{\text{A}}$, B, C,	Arithmetic unit	Enable arithmetic unit register A, B or C to write data onto the arithmetic unit data bus.

Table D Control Logic Output Signals

1.4 Circuit Diagrams

Most of the circuit diagrams have been laid out with groups of components which perform certain functions confined within imaginary blocks. The corners of the blocks are included in the drawing. The purpose of the blocks is to assist the reader to follow the functional paths throughout the system.

Some diagrams, notably those in the digital section, are not functionally divided. This is due to the nature of the signals within these boards making the functional tracing of signal paths a practical impossibility. Fault finding on these boards (pcb 2 - 5, 7, 8, 10 - 13 and 15 - 17) should not be attempted.

Immediately following this introduction is a chart showing the relation between these circuit diagrams and the printed circuit boards. The purpose of this chart is to provide the link between the functional circuit diagrams and the physical location of the components. It also indicates the major functional areas of the instrument.

List of Circuit Diagrams

1	1174 Relay Control	29	1172 Serialiser	59	Function Decode (2)
2	1170 Clock Dividers	30	1172 Pulse Shaper	60	Function Decode (3)
3	1170 Buffer Dividers	31	1170 Latch Store Control	61	Function Decode (4)
4	1170 Ramp Control	32	1170 Latch Store (1)	62	1170 Main Control Bd.
5	1174 Power Supply	33	1170 Latch Store (2)	63	1170 Main Control 'B' (1)
6	1174 Output Range Relays	34	1170 Latch Store (3)	64	1170 Main Control 'B' (2)
7	1174 Output Amplifier	35	1170 Latch Store (4)	65	1170 Main Control 'B' (3)
8	1174 Programmable Attenuator	36	1170 Latch Store (5)	66	Main Store
9	1174 Analogue Switching	37	Latch Store Output	67	Timing Counter & Marker Bit Generator
10	1174 1MHz Process	38	1172 Touch Key Latches (1)	68	Error Detection Logic Board 12
11	1174 20MHz Xstal Oscillator	39	1172 Touch Key Latches (2)	69	Equiv. Gates
12	1174 Xstal Offset	40	1172 Touch Key Latches (3)	70	Keyboard Control
13	1174 Phase Detector & V.C.O.	41	1172 Touch Key Latches (4)	71	Display Decode
14	1174 Input Relays & Buffer	42	1170 Power Input	72	D/A Mark/Space Generator
15	1174 Heterodyne/Overload Detector	43	1170 Earthy P.S.	73	Auto Range
16	1174 Reversible Counter	44	1170 Floating P.S.	74	Display Assy (1)
17	1174 D-A Shaper	45	1170 Sensing Amp.	75	Display Assy (2)
18	1174 Mother Board	46	Power Dist. (+5V)	76	Store State Indicator
19	1174 Amplitude Control	47	Power Dist. (+18V & -16V)		
20	1170 Input Circuit	48	Power Dist. (-11V & 0V)		
21	1170 Demod. & V to F	50	N Cycle Counter and Generator Divider		
22	1170 Bias Input Gen.	52	Heterodyne Logic		
23	1170 Bias Input Control	53	1170 Sin/Cos Generator		
24	1170 Bias Input Ranging	54	Sequence Logic		
25	1172 Strobe Gen.	55	Arith. Reg. A.		
26	Touch Keys (1)	56	Exp. Counter & Decode		
27	Touch Keys (2)	57	Iteration Counter		
28	Touch Keys (3)	58	Function Decode (1)		

Circuit 1 (1174 Board 1)

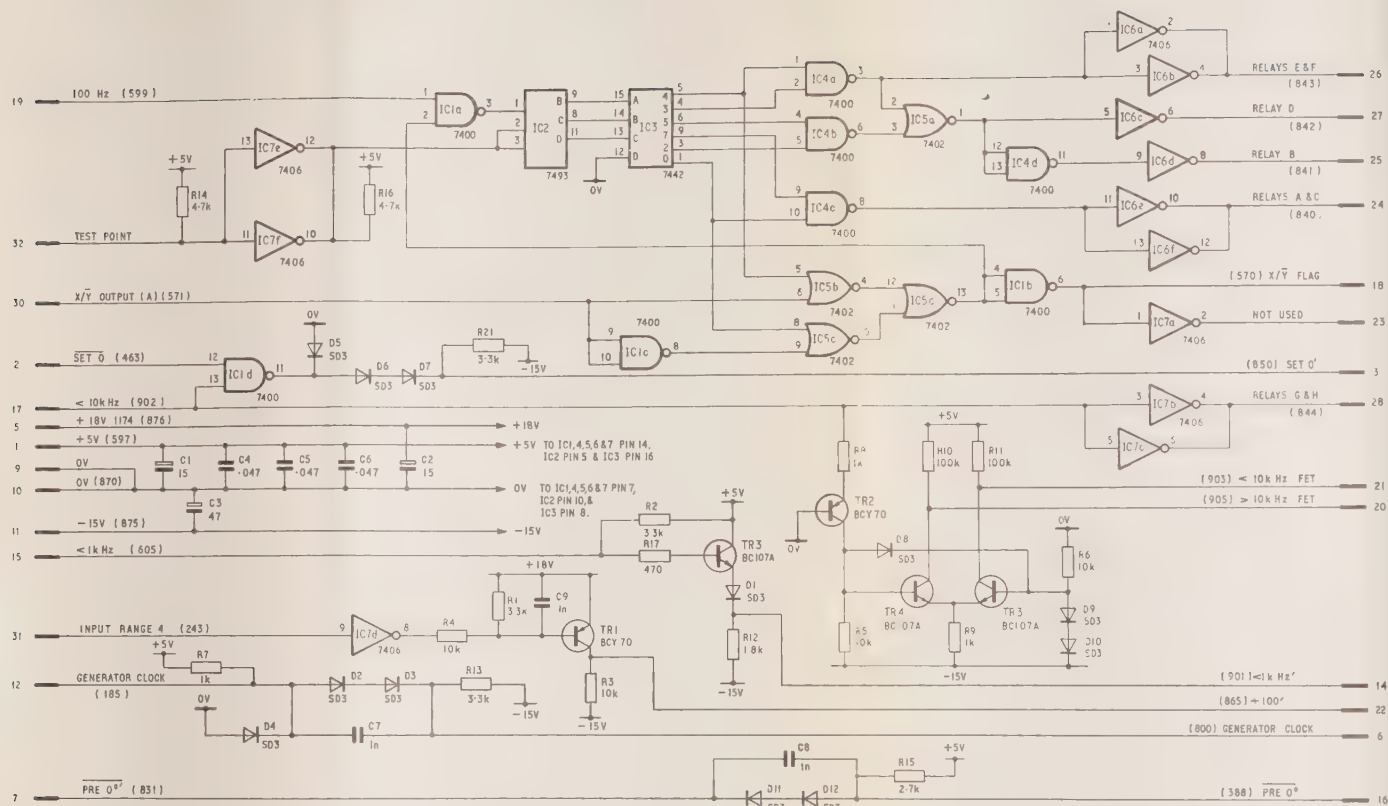
The circuitry on this board is used to control the switching sequence of the input amplifier relays on Board 14 (circuit 14) when changing channel, and to provide various driving signals.

The top part of the circuit is concerned with relay control. The $X/\bar{Y}$ input is a command from the mainframe which causes the relays to select the desired input channel and $X/\bar{Y}$ FLAG when high signals the mainframe that the selection process is complete. The outputs of IC3 go low one at a time in sequence as determined by the state of the counter IC2. The counter is disabled when measuring X only if the IC3 "0" output is low, and when measuring Y, only if the "4" output is low. In either of these stable states, the $X/\bar{Y}$ FLAG is high.

When measuring point-to-point, measurements on the X channel are made first, and the relay changing sequence is as follows.

X/Y	Low IC3 output	Relays closed	$X/\bar{Y}$ FLAG	Action
1	0	A,C,D	1	Measure X
0	(1)	D	0	} Change dummy loads
0	2	B	0	
0	3	B,E,F	0	
0	4	B,E,F	1	Relays in final state
1	5	B	0	Measure Y
1	(6)	D	0	} Change dummy loads
1	7	A,C,D	0	
1	0	A,C,D	1	Relays in final state
				Wait

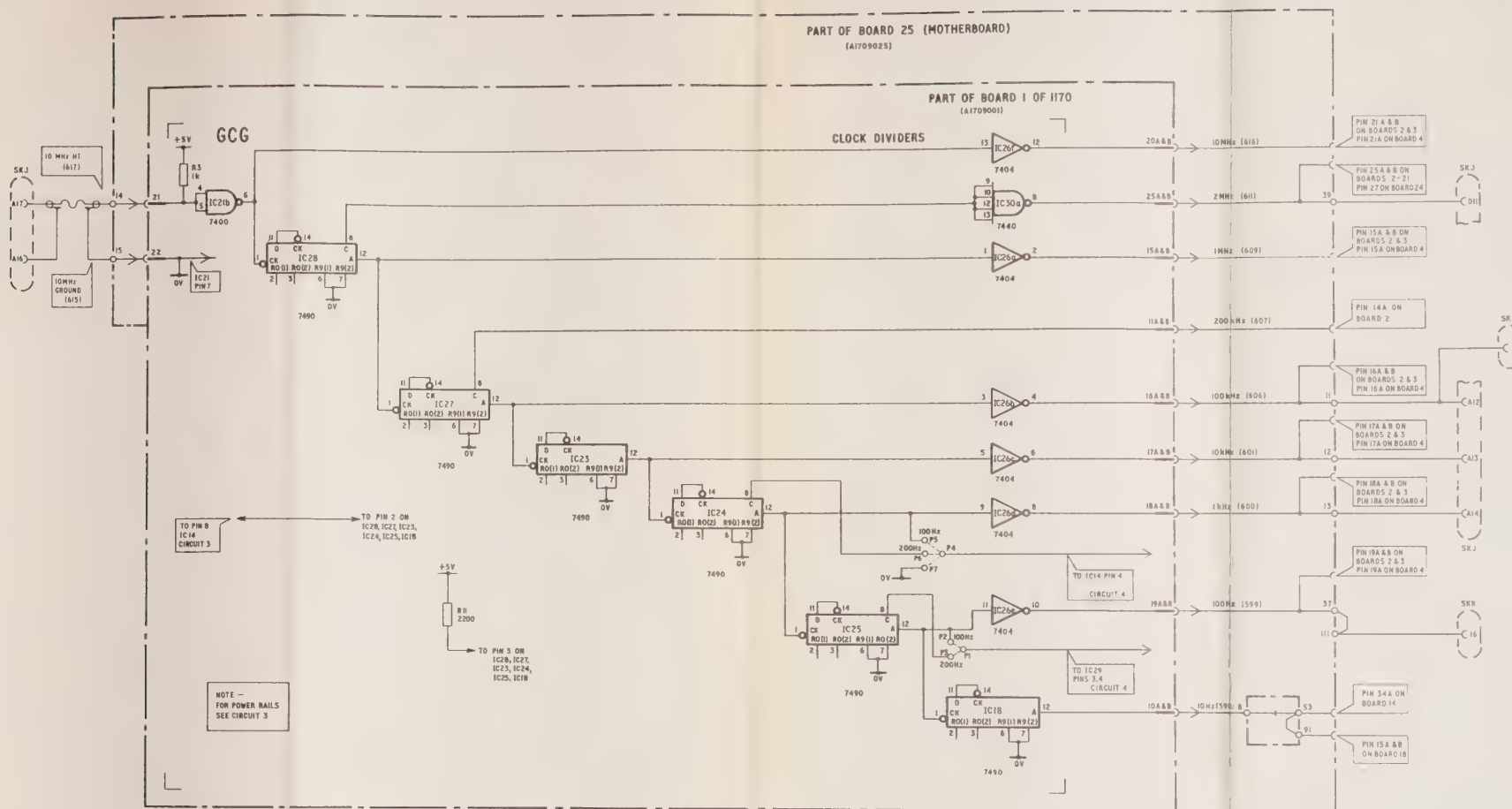
Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 1			CIRCUIT No. 1 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
50	185	52		842	14
73	243	14.20.63		843	14
	388	50		844	14
50	463	52		850	16
	570	14.64		865	14
14.62	571		5	875	18
2.14	599	50.54	5	876	18
50	605			901	16.17
	800	16	11	902	9
16	831			903	14
	840	14		905	14
	841	14			



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 2

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 2		
SOURCE	SIG No.	DESTINATION
1	615	
11	617	
	616	54
	611	21.25.50.54.58.65.66.69.70.72
	609	54
	607	50
	606	5.54.44.
	601	12.50.54
	600	12.50.54
	599	1,14,50,54
	598	73.



SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2

Circuit 3

The MOS store data output lines (339 to 342) define the frequency required from the synthesiser output in circuit 1. These data are loaded into the counters (IC10 etc.) which are then counted down by the 10.2 to 12MHz output from circuit 13. If the synthesiser output is correct the outputs to circuit 4 will be 100Hz; or higher or lower if not.

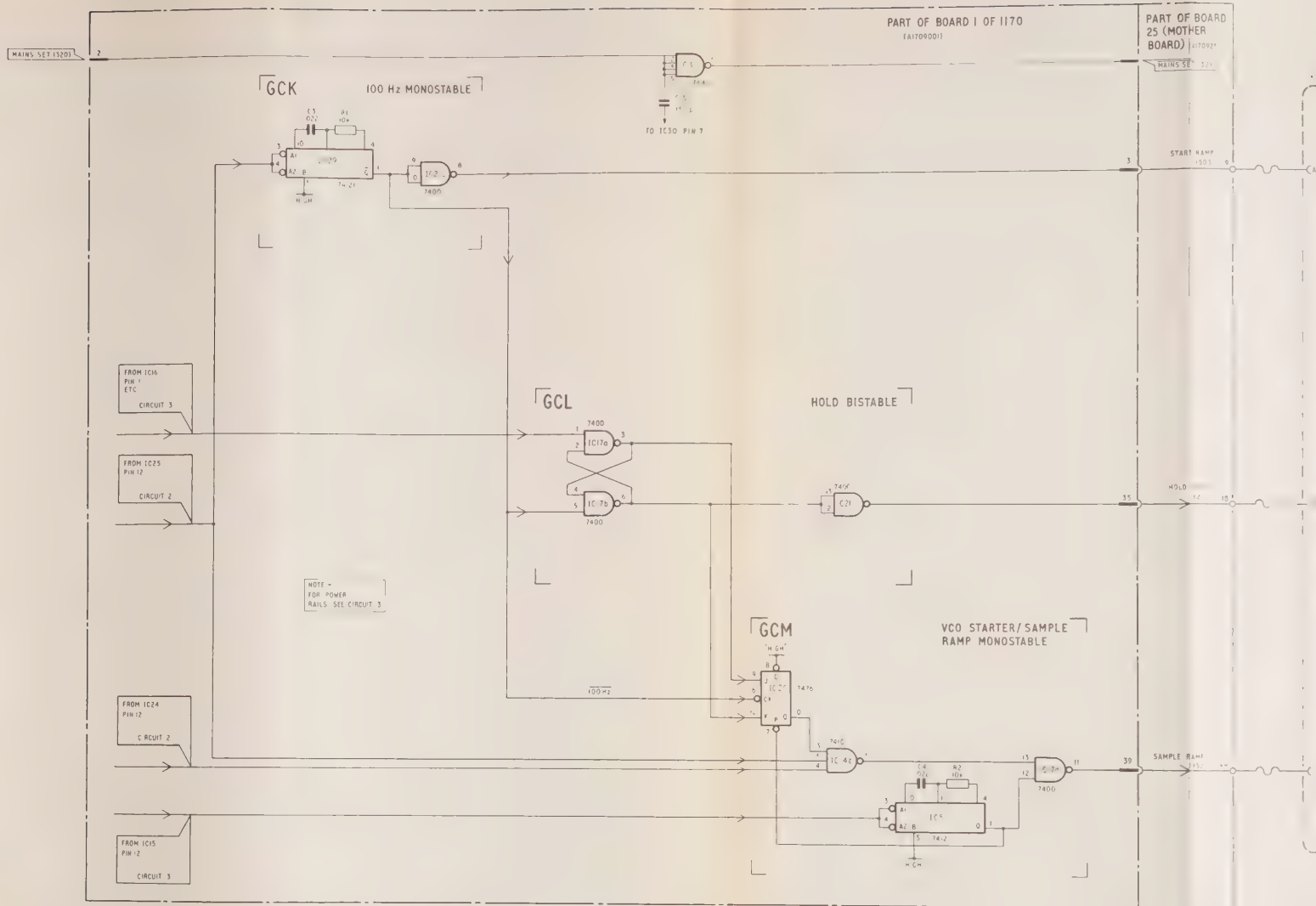
Outputs 359, 360 and 26 are related to the generator circuit (14) and not to the synthesiser circuits as are the other signals. Output 36 is not used in the 1174.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 3		
SOURCE	SIG No.	DESTINATION
13	619	
	620	
	612	
66	339	50.63.69.70.71.72.74.
66	340	50.63.70.71.72.74.
66	341	50.63.70.71.72.73.74.
66	342	50.63.70.71.72.74.
69	170	
67	542	69
67	543	69
69	358	
69	13	
	359	6
	360	6
	26	
	640	
	642	
	688	
	643	
	644	
	689	

Circuit 4

This circuit provides the three pulse outputs used in circuit 5. See "Introduction to the Generator" for a description of the timing and use of these signals.

Interconnections		
Signal numbers are as in Section 2.4.		
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 4		
SOURCE	SIG No.	DESTINATION
44	320	
	321	30.34.50.58.66.
	503	13
	211	13
	452	13



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 5 (1174 Board 5)

The supplies of the 1174 are non-floating and with the exception of the +5V level are derived from the mainframe +18V rail, by means of a synchronised self-oscillating inverter using a ferrite transformer. The +18V rail is itself also used in the 1174.

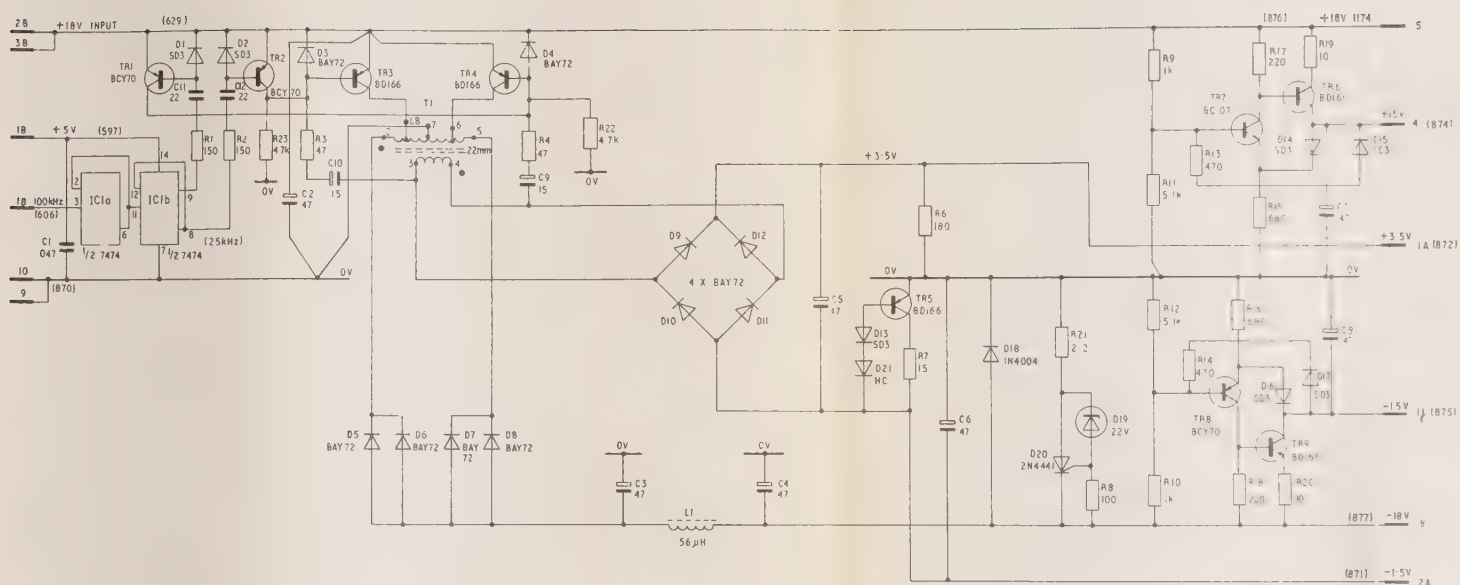
TR3 and TR4 alternately switch +18V to their respective collector connections on the transformer. Positive feedback is provided from the secondary and oscillations are synchronised to 25kHz by transistor switches TR1 and TR2.

The -18V rail, obtained by autotransformer action, is "crowbar" protected against overvoltage and is protected against voltage reversal.

The +15V and -15V rails are derived from their respective 18V rails by use of feedback-pair current-limited voltage stabilisers.

The transformer secondary output is bridge-rectified to provide a 5V potential difference. The negative rail is held by transistor TR5 at -1.5V with respect to 0V, and thus +3.5V becomes the voltage of the positive rail. These rails are used for the reversible counter logic on Board 2.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 5		
SOURCE	SIG No.	DESTINATION
43.46	597	18
2	606	44.54
43.47	629	
	871	16
	872	16.17
	874	4.7.8.9.10.12.13.14.15.17
	875	1.4.7.8.9.10.13.14.15.17
	876	1.6.7.14
	877	6.7.14



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

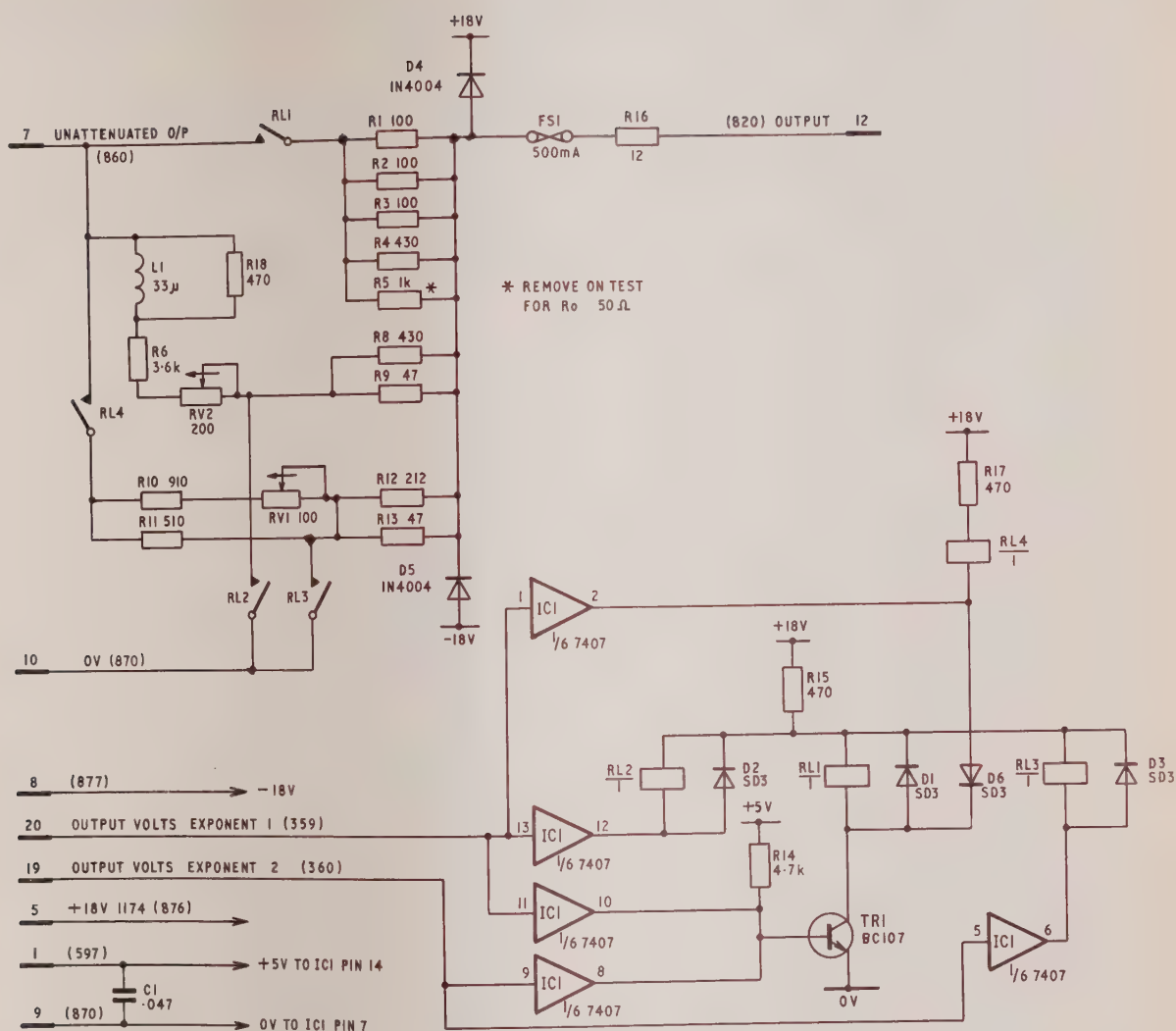
Circuit 6 (1174 Board 6)

The circuitry on this board is used for all frequencies. The low-impedance high-level UNATTENUATED OUTPUT signal comes from Board 7, and with relays closed according to the table below, is attenuated by the required factor for the desired output range, and brought up to the required impedance. The output range is determined by the signals OUTPUT VOLTS EXPONENT 1 and OUTPUT VOLTS EXPONENT 2 (abbreviated to OVE 1 and OVE 2 for the purposes of the table).

Output Voltage range	OVE 1	OVE 2	Relays closed
10–100mV	High	Low	3
0.1–1V	Low	High	2, 4
1–10V	High	High	1, 4

The signal leaves this board and passes via a 5MHz 50 ohm filter to the Generator Output connector.

Interconnections		
Signal numbers are as in Section 2.4.		
Sources and destinations are circuit diagram numbers: if none shown all connections are within this circuit.		
CIRCUIT No. 6		
SOURCE	SIG No.	DESTINATION
3	359	
3	360	
	820	
7	860	
5	876	18
5	877	18



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 7 (1174 Board 7)

This circuit is a high-power operational amplifier with nominal gain of -5 (taking into account the effect of the signal source impedance) and output impedance of 10Ω . It is used throughout the frequency range, and is direct coupled.

TR1 and TR2 form a long-tailed pair, the base of TR1 having feedforward from the virtual earth via C14, and IC1 itself around its input stage via C13. TR3 and TR4 and their associated circuitry are constant current sources. TR5, having its base clamped, operates as a current-mirror and feeds the common-collector stage TR6.

The output stage consists of the power transistors TR7 – TR10. These are biased in Class AB, transistors TR7 and 10 conducting at low output levels and TR8 and 9 only conducting for higher levels.

Interconnections		
Signal numbers are as in Section 2.4.		
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 7		
SOURCE	SIG No.	DESTINATION
	860	6
5	874	18
5	875	18
5	876	18
5	877	18
8	900	

Circuit 8 (1174 Board 8)

This board accepts the constant amplitude generator sinewaves, from either the high or low frequency sources on Board 9. This signal is modified in amplitude by a programmable-gain amplifier and is fed off the board to the output amplifier.

The "O/P V (DC)" command input to the board on edge connection 15 comes from Board 4 and is a positive d.c. voltage level proportional to the desired output voltage of the instrument (ignoring the decimal multiplier). This level is attenuated by the R19 to 22 combination and further by the loading effect of the field-effect transistor TR1B on the output impedance of R19-22.

In a similar way the output of IC1 is attenuated by the R16, R10, R11 combination and by the loading of the f.e.t. TR1A on its output impedance. The output impedance of the two sets of resistors are equal, and the drain-source resistances of the two f.e.t.s are equal since they are a matched pair and have their gates driven by the same signal.

Pin 3 of IC2 is held at about +39mV and the gate drive of TR1B adjusts itself so that whatever level of the command "O/P V (DC)", the command voltage is attenuated to be also +39mV at pin 2 of IC2. The attenuations of IC1 output is its feedback path (and thus the gain of the IC1 stage) and that of "O/P V (DC)" to the standard level of 39mV closely follow one another, and the sinewave output of the board is thus directly proportional (exponent excepted) to the "OP V (DC)" command.

IC3 is connected as an inverting, unity gain amplifier and thus the d.c. offsets to the inputs of IC1 and IC2 caused by current through the potential divider chains on the gates of TR1A and TR1B are cancelled by equal and opposite offsets caused by currents through R7 and R26 respectively.

Interconnections		
Signal numbers are as in Section 2.4.		
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 8		
SOURCE	SIG No.	DESTINATION
9	821	
9	822	
19	823	
9	851	
17	873	9
5	874	18
5	875	18
	900	7

Circuit 9 (1174 Board 9)

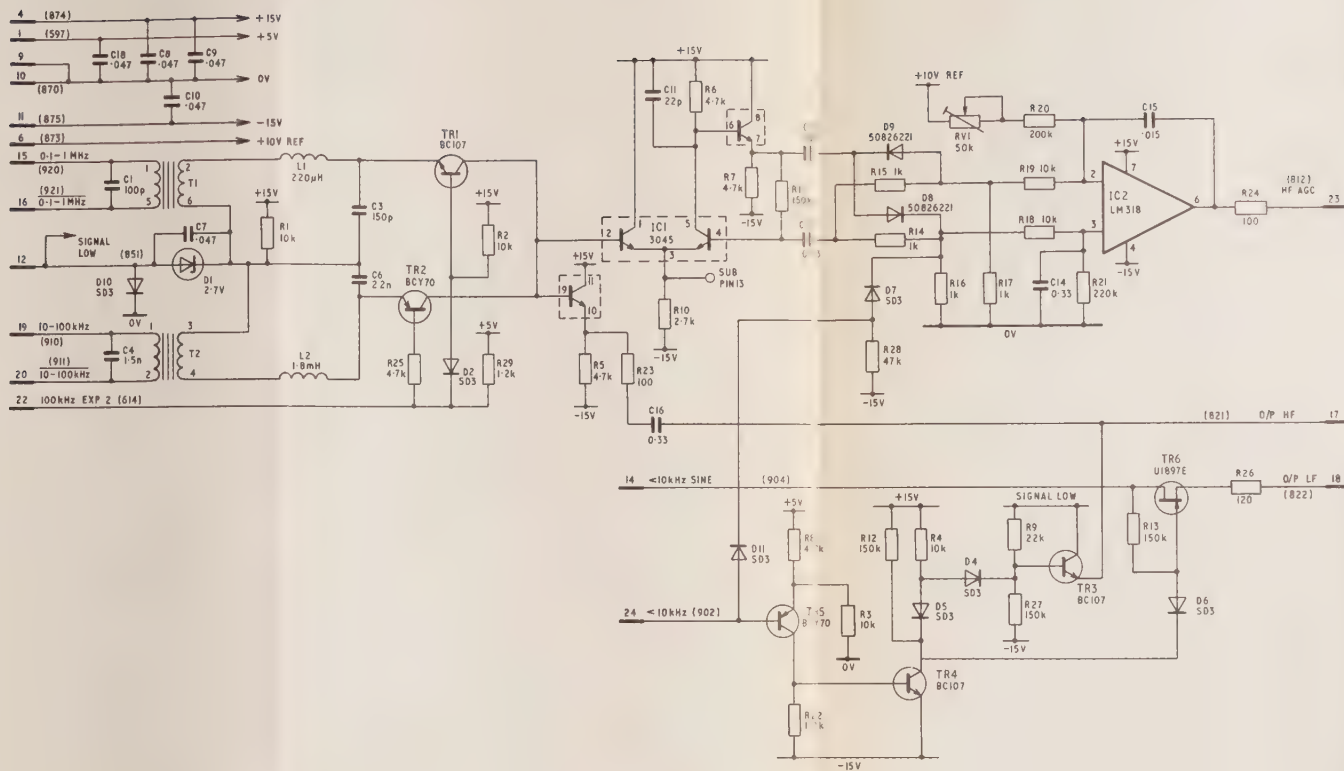
When the 1174 output frequency is between 10kHz and 1MHz, a signal at this frequency from Board 10 appears between edge connections 19 and 20 or 15 and 16. It is converted from differential to single ended form and bandpass filtered by a transformer and surrounding circuitry, and is applied to IC1 pin 9.

On either of the above ranges, the “< 10kHz” input is low. The shunt switch TR3 and the series switch TR6 are both opened, and the signal leaves the board on “O/P HF”.

The remainder of IC1, and IC2 and associated circuitry form a mean-modulus level measuring system, operative for the two top frequency ranges only. The three IC1 transistors form a differential amplifier, whose bias point is stabilised by the d.c. negative feedback through R11. The a.c. feedback applied to IC1 pin 4 through C13 is approximately equal to the voltage on pin 2, and this condition dictates that the potential difference between the anode of D9 and the cathode of D8 is the modulus of the voltage on IC1 pin 2. The output of IC2, HF AGC, responds by ramping negative if the signal is smaller than the value predetermined by the setting of RV1, and positive otherwise. HF AGC is fed back to Board 10 to control the amplitude of the signal on the two top frequency ranges.

When the 1174 output frequency is below 10kHz, a digitally generated sinewave from Board 4 appears on edge connection 14 (< 10kHz SINE), and the < 10kHz signal is high. Its application through D11 simulates the application to the HF AGC system of a large signal. The HF AGC output ramps fully positive and cuts off the high-frequency signals from board 10. The switches TR6 and TR3 are both turned on. The signal leaves on O/P LF, and is combined with that on O/P HF in a resistive network on Board 8. Frequency-dependent loading of this network by components on the present board is avoided, and remaining high frequency signal or noise removed, by grounding the O/P HF line with transistor TR3.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 9			CIRCUIT No. 9		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
50	614	10.11.12	11	902	1
	812	10	19	904	
	821	8	10	910	
	822	8	10	911	
17	851	8	10	920	
	873	8	10	921	
5	874	18			
5	875	18			



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 10 (1174 Board 10)

This board originates the instrument's output signal on the two top frequency ranges.

The signals at 10MHz and 1MHz presented to edge connections 14, 17 and 18 have been obtained by division of the 20MHz master crystal. The 1MHz signal is switched off however when not required. Each of the two pairs of transistors driven by these signals produce pulses of current into its collector R-C filter circuit, the pulse size being determined by the HF AGC line. The smoothed output of each filter is buffered and feeds a resonating L-C circuit. The two L-C circuits thus produce controllable amplitude sinewaves at fixed frequencies of 1 and 10MHz having low harmonic content.

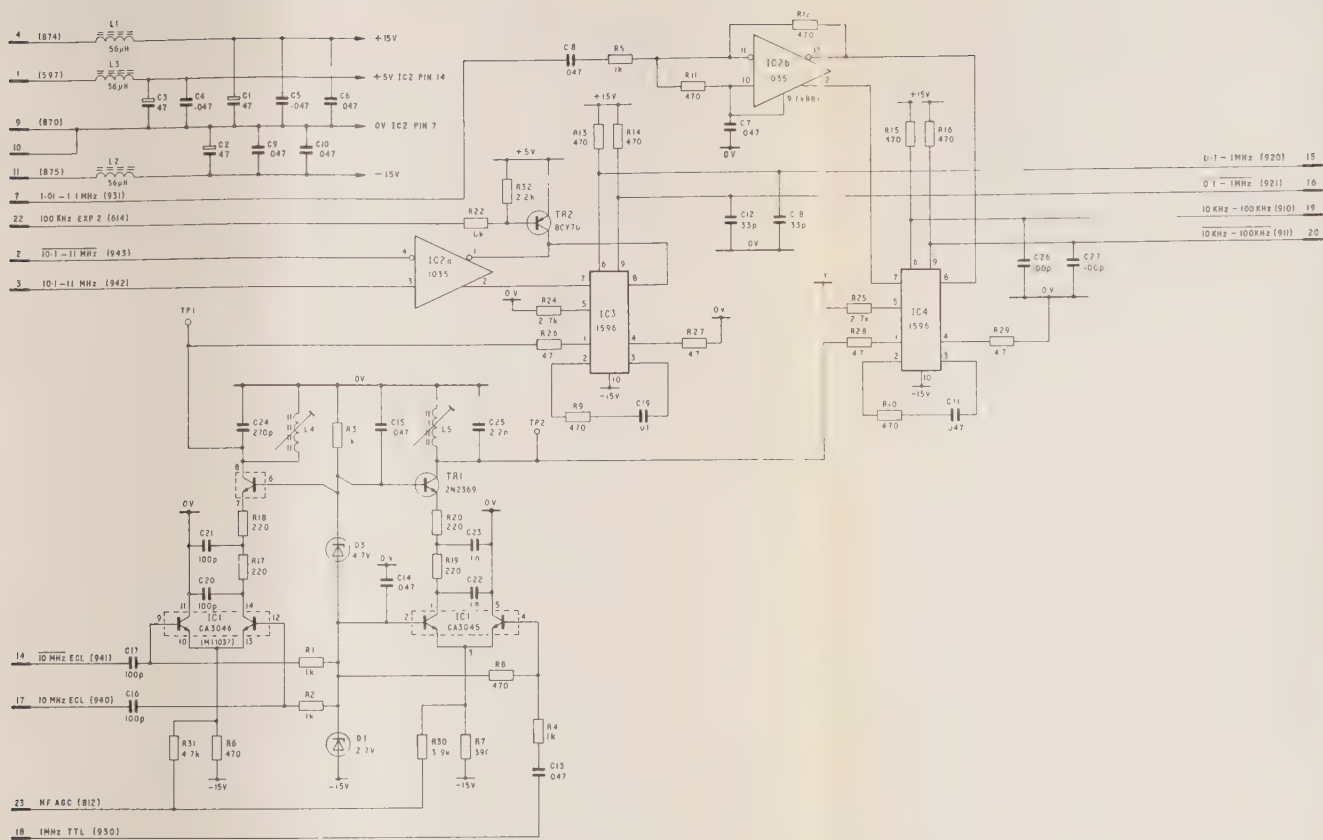
The input squarewave signals 1.01 – 1.1MHz and 10.1 – 11MHz are derived by division of the 20.2 – 22 voltage-controlled oscillator on Board 13.

The balanced modulator IC4 is thus presented with a squarewave at 1.01 – 1.1MHz and a sinewave at 1MHz. Its output signal has a spectrum which is predominantly 10 – 100kHz (the wanted frequency), and does not contain a high proportion of low order harmonics, since one of the modulator inputs is a pure sinusoid.

In a similar way IC3, being presented with a squarewave at 10.1 – 11MHz and a sinewave at 10MHz produces a 100kHz – 1MHz signal which also has no low-order harmonics. This signal is disabled when not required, by the 100kHz EXP 2 line.

These two signals are made available to Board 9, where the upper sideband of each is filtered off.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 10			CIRCUIT No. 10		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
50	614	9.11.12	11	930	
9	812		11	931	
5	874	18	11	940	13
5	875	18	11	941	13
	910	9	13	942	11
	911	9	13	943	11
	920	9			
	921	9			



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 11 (1174 Board 11)

On this board is the 20MHz master crystal oscillator to which all major timing signals in the instrument are locked. A 10MHz signal goes to a divider chain within the mainframe to provide clocks for the logic.

The 10.1 – 11MHz e.c.l. signal (input to this board) is converted to t.t.l., divided by ten in frequency, but is disabled for the top frequency range.

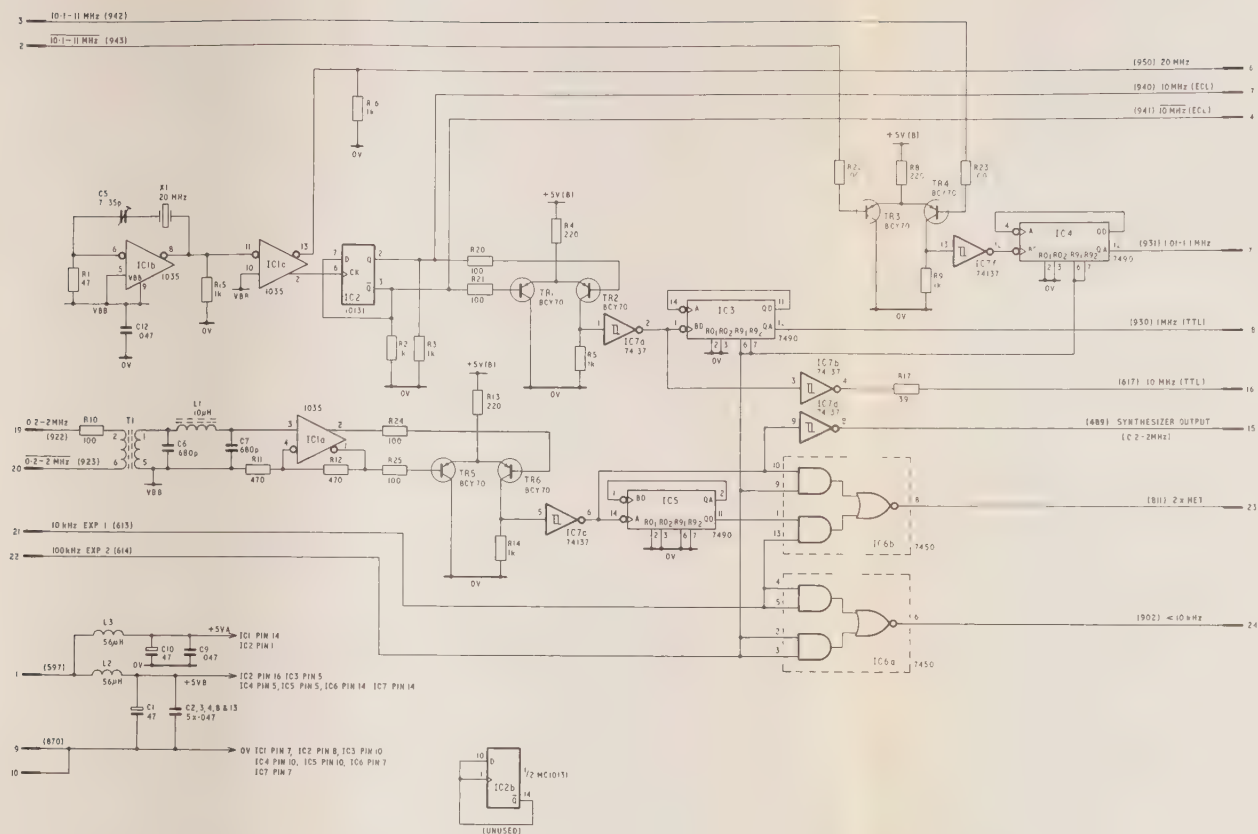
The 0.2 – 2MHz (nominal) signal is bandpass-filtered (chiefly to remove its upper sidebands above 20MHz), is followed by an e.c.l. schmitt, and is converted to a t.t.l. signal. Gating and (if necessary) frequency division of this signal is employed to generate the 2 X HET signal, which has the following frequencies:

Instrument frequency range	2 X HET frequency
100 – 999.9 kHz	198 – 1997.8 kHz
10 – 99.9 kHz	18 – 197.98 kHz
all other ranges	signal absent

These frequencies are divided by 2 on Board 12 and the resulting signal (1kHz below the instrument measuring frequency) is used to heterodyne with the instrument input signal, resulting in a constant 1kHz signal for analysis.

The SYNTHESIZER OUTPUT signal (always between 0.2 and 2MHz) is used on the frequency ranges below 10kHz within the mainframe only where it provides the generator clock and drives the correlator.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 11			CIRCUIT No. 11 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
50	489	50		930	10
	613	12		931	10
	614	9.10.12		940	10.13
	617	2		941	10.13
	811	12	13	942	10
	902	1.9	13	942	10
12	922			950	12
12	923				



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 12 (1174 Board 12)

The circuitry on this board is largely concerned with generation of the HET signal, which is used solely within the input system on the top two frequency ranges. On these ranges the HET signal is always exactly 1kHz below the measurement frequency and is used to heterodyne input signals to 1kHz for measurement by the correlator.

The two crystal oscillators have frequencies of 20.002 MHz (only enabled for the 100 – 999.9 kHz range) and 20.02 MHz (only for the 10 – 99.99 kHz range). When in use an oscillator is phase locked with an offset to the 20 MHz master crystal oscillator on Board 11. First the chosen oscillator's output is mixed with 20 MHz by IC3 section C (pins 12–15), is filtered, and the resulting frequency of 2 or 20 kHz respectively is divided by two. This is phase-locked to a reference frequency of 1 or 10 kHz, also derived from the 20 MHz master oscillator.

One of the above two crystal frequencies (or 20MHz for frequency ranges below 10kHz) is mixed with the v.c.o. signal on edge connection 12 and the 0.2 – 2MHz signal which results will have frequency ranges as follows.

Instrument frequency range	0.2 – 2MHz (nominal) frequency
100 – 999.9kHz	198 – 1997.8kHz
10 – 99.99kHz	180 – 1979.8kHz
below 10kHz	200 – 1999.8kHz

For the lower frequency ranges the signal is buffered on Board 11 and is only used in the mainframe. For the two top ranges the signal is only used by the 1174 plug-in. For the top range it is divided in frequency by 2, and for the next range by 20, to form the HET signal used on Board 15.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connectors are within this circuit.		
CIRCUIT No. 12			CIRCUIT No. 12 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
2	600	50.54		922	11
2	601	50.54		923	11
50	613	11	11	950	
50	614	9.10.11	13	951	
	810	14.15			
11	811				
5	874	18			



Circuit 13 (1174 Board 13)

This board is responsible for generating the 20.2 – 22MHz signal and associated signals.

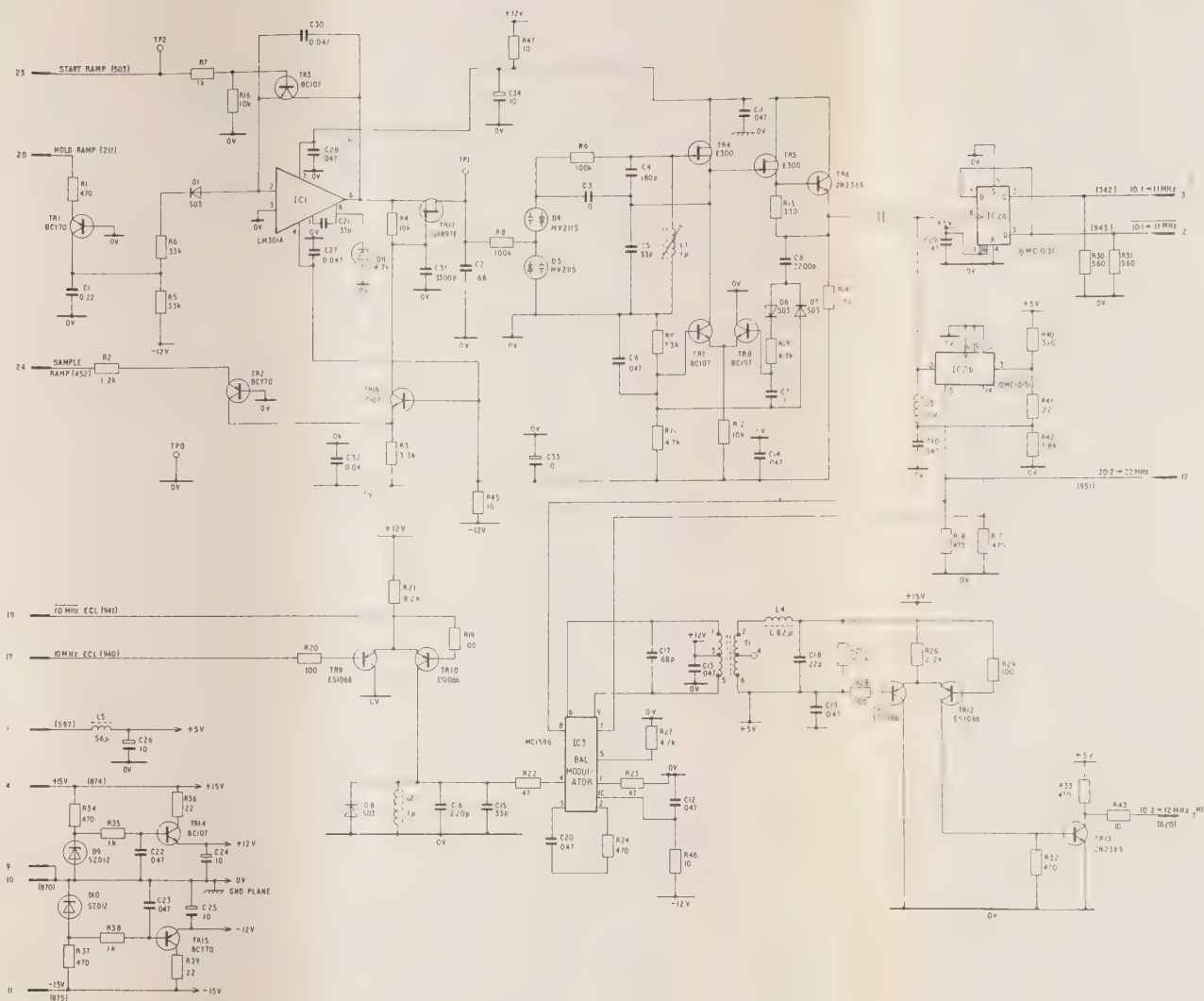
TR4 – 8 and their circuitry form a Colpitts oscillator running at frequencies between 20.2 and 22MHz. It is phase locked to the master oscillator on Board 11, the loop having a programmable divider within the 1170 mainframe (Board 1) and a phase detector which consists of a sample-and-hold system with IC1 as integrator. Using the three signals START, HOLD, and RAMP, a direct voltage is established on C2, and this is used to tune the oscillator with varactor diodes D4 and D5. For a description of the phase-locking mechanism, see the section within the text entitled “Introduction to the Generator”.

TR4 source current, and hence the amplitude of the oscillator output through C9, is controlled by TR7, TR8 and the level-sensing diodes D6 and D7.

The 1174 generator output is derived from the 20.2 – 22MHz signal on all frequency ranges by frequency changing and division. The two top range frequencies, 100 – 999.9kHz, and 10 – 99.99kHz, are derived on Board 10. The generator output on all lower ranges is derived by digitally constructing a sinewave. The circuitry on Boards 2, 3, and 4 is concerned with this.

IC3 and the associated circuitry form a mixing circuit for deriving the 10.2 – 12MHz signal required by the programmable divider within the loop.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 13			CIRCUIT No. 13 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
4	211	3	11	911	10
4	452			932	10.11
4	503			943	10.11
	620			95	12
5	874	18			
5	875	18			
11	940	10			



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 14 (1174 Board 14)

This board accepts signals selected in turn from the two input connectors on the instrument front panel. The signal is fed through the attenuator system and is buffered by IC1. In combination with Board 15, input signals are heterodyned to 1kHz on the top two frequency ranges.

Relays A to F are concerned with selecting which of the two front panel input connectors is connected to the input amplifier at any one time. For details of the switching sequence of these relays during the measurement process, see the description for Circuit 1. Whichever input is not currently being used for measurement has a dummy load of 1MΩ connected to earth.

This board and Board 15 work closely together on frequency ranges of 10kHz and above. Relays G and H are open and the inputs thus become capacitively coupled. The signal is attenuated if necessary, is buffered by IC1, and is fed to Board 15 pin 1. TR 3 has a high impedance. The signal is heterodyned by circuitry on Board 15 to a constant 1kHz and is fed back via Board 15 pin 3, buffered by IC2 and passed via PLK to the mainframe (Board 24).

For frequencies below 10kHz, the inputs are direct coupled. TR3 is switched on, and the output switch on Board 15 switched off. The signal is therefore not heterodyned but passes directly to the output buffer IC2 and then to the mainframe.

The input circuitry to IC1 will either pass input signals to IC1 without attenuation, with RLJ closed, and TR1 and TR2 open, or will attenuate input signals by a factor of 100 with RLJ open and TR1 and TR2 closed.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 14			CIRCUIT No. 14 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
24	236	20	1	844	
73	243	1.20.63	1	865	
21	260	73	5	874	18
1	570	64	5	875	18
62	571	1	5	876	18
2	599	1.50.54	5	877	18
12	810	15	1	903	
1	840		1	905	
1	841				
1	842				
1	843				

Circuit 15 (1174 Board 15)

This board is not used below an instrument operating frequency of 10kHz. At such frequencies the output switch TR4 is turned off. Above 10kHz the balanced modulator IC1 has two inputs: BUFFERED INPUT SIGNAL (at the input operating frequency) and HET (at 1kHz below the operating frequency). Production of the HET signal is described for Circuit 12. The output of the modulator is a constant 1kHz, with amplitude related to that of the input signal.

IC2 filters and buffers the 1kHz signal. Provision is made for gain adjustment by means of RV1, and the signal is passed via TR4 back to Board 14.

Interconnections

All connections on this circuit (Board 15) are made to Circuit 14 (Board 14) via the 8-way connector.

Circuit 16 (1174 Board 2)

This circuitry is used in the generation of the output sinewave for frequencies below 10kHz.

ICs 5, 6, and 7 form a reversible counter. The GENERATOR CLOCK' input is at a frequency of 2000f for f below 1kHz, and 200f for f between 1 and 9,999kHz, where f is the measurement frequency. The counter counts up and down (as determined by the UP/DOWN bistable, IC 11b) twice during one measurement frequency period, the first time with the POLARITY output high and the second time with it low. To achieve this, counts of 500 and 50 are used for below and above 1kHz measurements respectively. The PRE 0⁰' output is normally high, and only goes low on the penultimate GENERATOR CLOCK' pulse. It is used within the mainframe, for the purposes of synchronising the correlator system.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers ; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers ; if none shown all connections are within this circuit.		
CIRCUIT No. 16			CIRCUIT No. 16 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
1	439	17		831	1
	440	17	1	850	
	441	17	5	871	
	442	17	5	872	17
	443	17	1	901	17
	444	17			
	445	17			
	446	17			
	447	17			
	448	17			
	800				
	830	19			

Circuit 17 (1174 Board 3)

This board is only used for frequency ranges below 10kHz, and, together with circuitry on Board 4, is responsible for generating a sinewave at the instrument output frequency on these ranges.

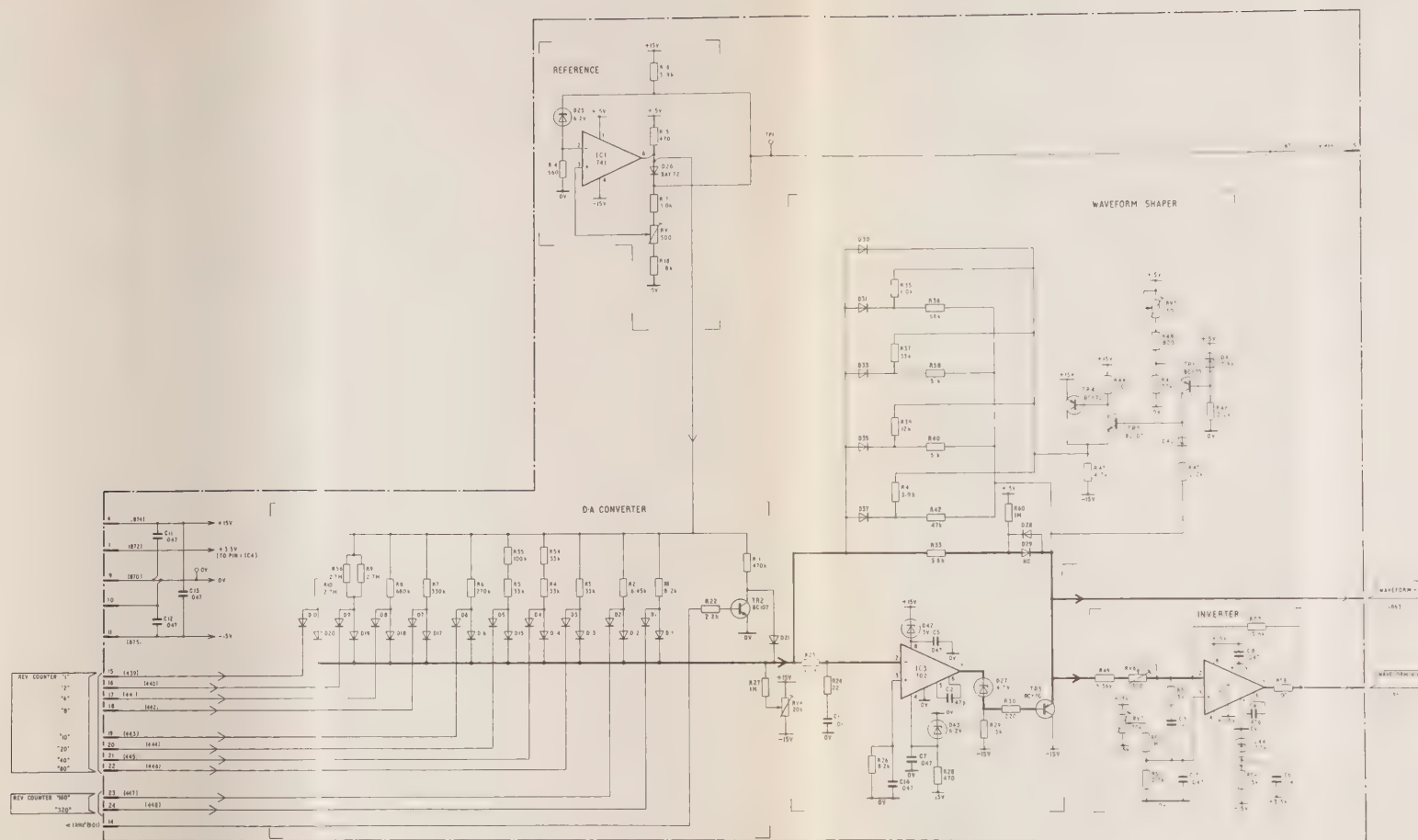
Edge connections 15–24 are driven by the parallel digital outputs of the reversible up-down counter on Board 2. This counter counts up and down twice during one period of the sinewave to be generated. Its output levels are approximately 1.5V more negative than TTL levels.

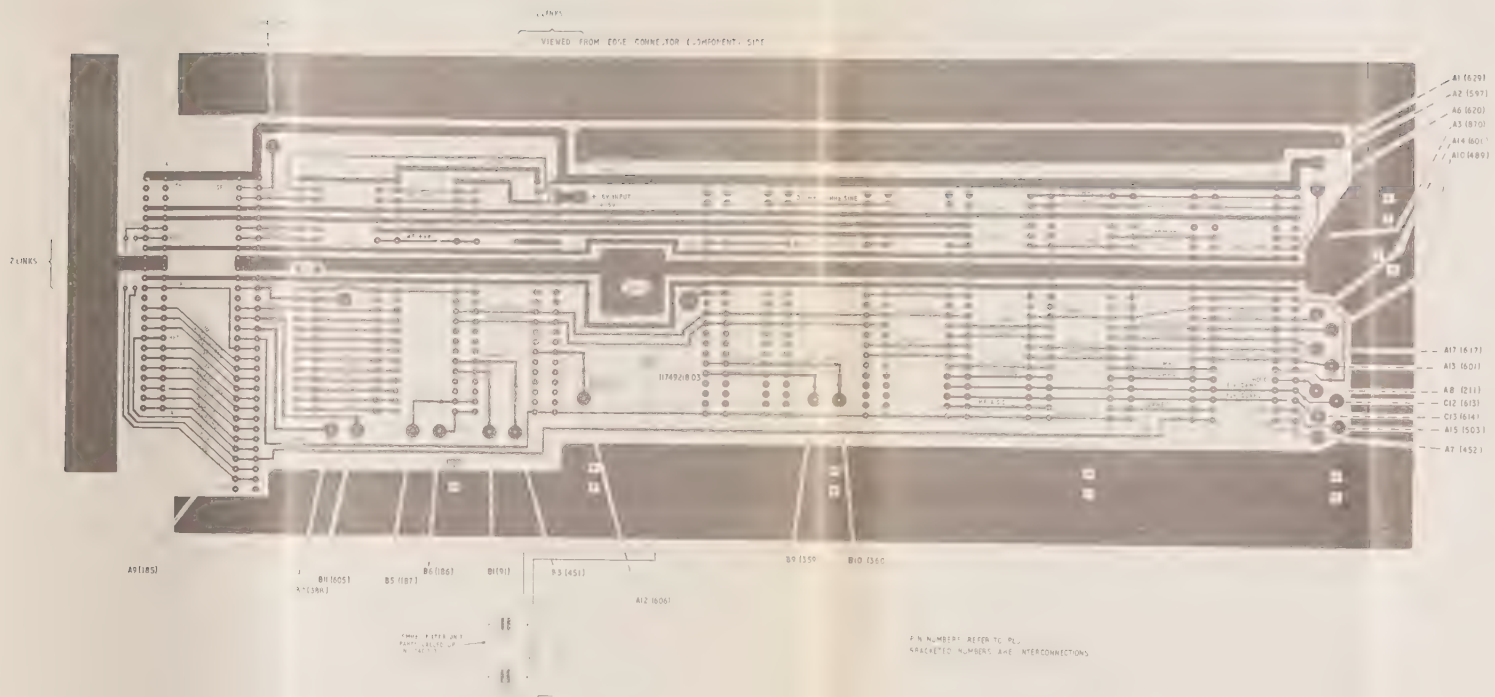
IC1 generates a +10.6V reference level (and a +10V level for use on Boards 8 and 9) using a precision voltage-reference diode in a bridge circuit. IC3 is connected as a virtual-earth amplifier, and the sum of the currents flowing into the virtual earth through diodes D11 to D21 must also flow through the feedback components. Each of these currents is determined in size by the resistance in series with the diode and can be diverted if its respective input from the counter is low. The net result is a unidirectional virtual-earth current which staircases up and down linearly twice during one period.

The voltage waveform on TR3 emitter is similar in shape to a negative-going full-wave-rectified sinewave. The feedback components have a non-linear current/voltage relationship and the voltage waveform is such as to give the required staircasing virtual-earth current. The output waveform is displaced from zero by the drop across D29 to allow for a similar but opposing drop by diodes on Board 4.

The output of the inverter IC4 circuit and IC3 are both fed to Board 4 for further processing.

Interconnections			Interconnections		
All connections on this circuit (Board 15) are made to Circuit 14 (Board 14) via the 8-way connector.			All connections on this circuit (Board 15) are made to Circuit 14 (Board 14) via the 8-way connector.		
CIRCUIT No. 17			CIRCUIT No. 17 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
16	439		16	448	
16	440			862	19
16	441			863	19
16	442		5	872	16
16	443			873	8,9
16	444		5	874	18
16	445		5	875	18
16	446		1	901	16
16	447				





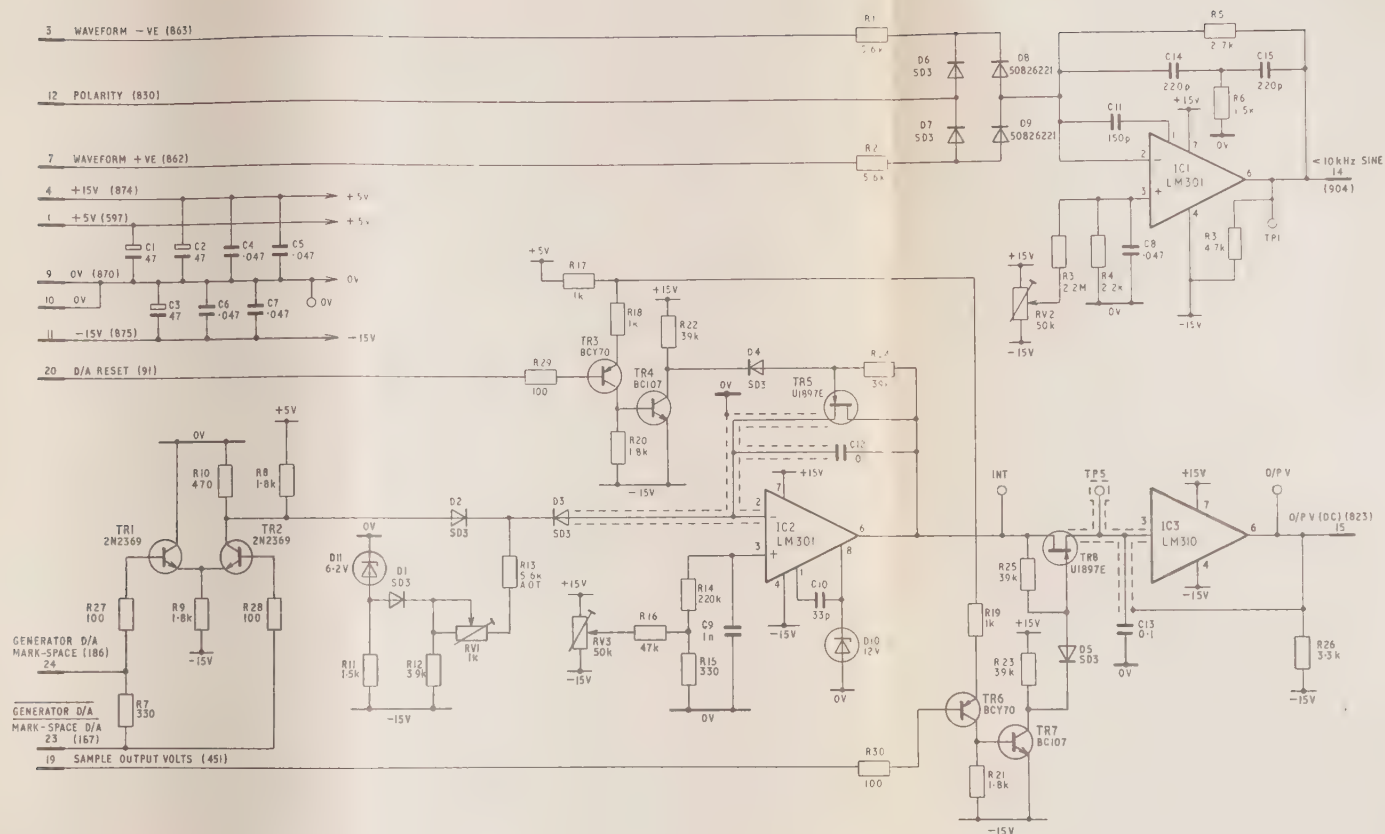
Circuit 19 (1174 Board 4)

This board has two separate functions. One part reconstitutes the two waveforms from Board 3 into a full sinewave, and the other decodes information from the mainframe to obtain the control voltage, proportional to the desired instrument output voltage, used by the programmable attenuator.

The POLARITY input, coming from logic using a -1.5V lower power rail, swings above and below 0V and biases diodes D8 and D9 off alternately during each successive half-cycle of the sinewave. The sum of the D8 and D9 currents is sinusoidal. IC1 is connected as a low-pass amplifier and provides some high-frequency filtering. Its output is a constant amplitude sinusoidal voltage and is fed to Board 9 for switching.

The generation of the “O/P V (DC)” level is achieved by means of a sample-and-hold system involving the three mainframe logic signals RESET, MS (mark-space), and SAMPLE. IC2 is an integrator, the output of which resets to zero when RESET is high. The MS and $\overline{\text{MS}}$ pair of signals are push-pull. When MS is low the integrator output ramps positive at a constant rate, adjustable by means of RV1. After a RESET pulse, there are three groups of low MS pulses, the first group being low for a time proportional to 100X the most significant digit of the Output Volts value in the 1170 MOS Store, and the second and third proportional to 10X and 1X the second and third digits respectively. After the final group the output voltage of the integrator is therefore proportional to the desired instrument output voltage (without regard to the decimal multiplier), and when SAMPLE goes high, is stored on the capacitor C13 and buffered by IC3 (a unity-gain voltage follower) for use as the “O/P V (DC)” signal. This is fed to the programmable attenuator on Board 8.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers: if none shown all connections are within this circuit.		
CIRCUIT No. 19		
SOURCE	SIG No.	DESTINATION
72	91	8
72	186	
72	187	
72	451	
	823	
16	830	
17	862	
17	863	
5	874	18
5	875	18
	904	9



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 20

A two stage attenuator and amplifier circuit. The first stage is a switched attenuator of X1, X0.1 or X.001 followed by an amplifier of X10 (no bias reject). The second stage is a switched attenuator of X1 or X0.1 followed by an amplifier of X10 (normal).

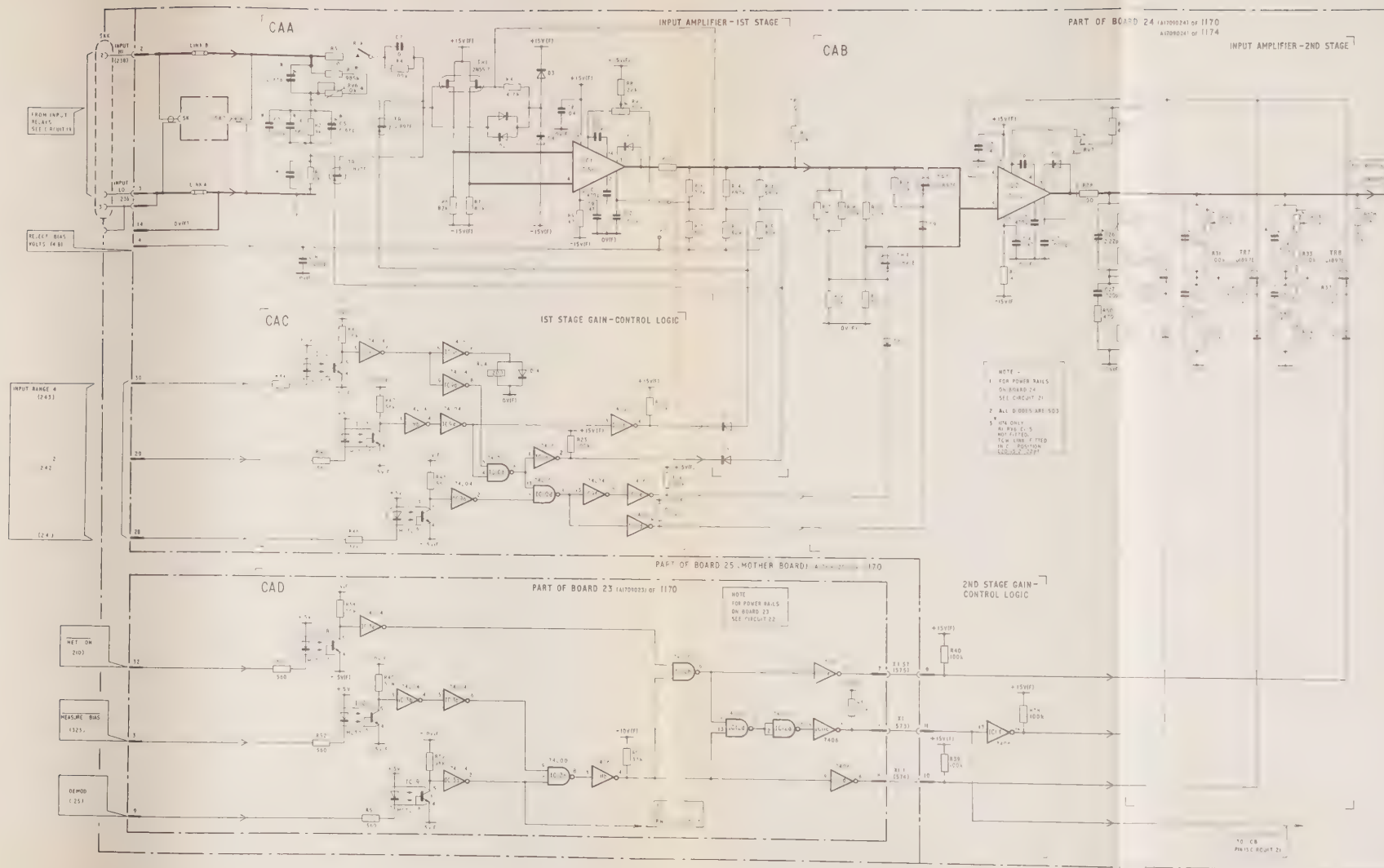
Range selection is as follows:-

	1st Atten.	2nd Atten.	Overall gain
10mV	X1	X1	100
100mV	X1	X0.1	10
1V	X.01	X1	1
10V	X.01	X0.1	0.1
100V	X.001	X0.1	.01

In addition the first amplifier gain is varied by the bias reject input (418). This is a variable voltage from the bias reject circuit, No. 24.

The second amplifier gain is altered from X10 to X11 or X16 depending on the selections of inputs (210), (323) and (125).

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 20		
SOURCE	SIG No.	DESTINATION
34	125	52
62	323	50.52.56
50	210	52
73	241	65
73	242	63
73	243	63
24	418	
14.24	236	
14	238	
	575	
	573	
	574	



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2.

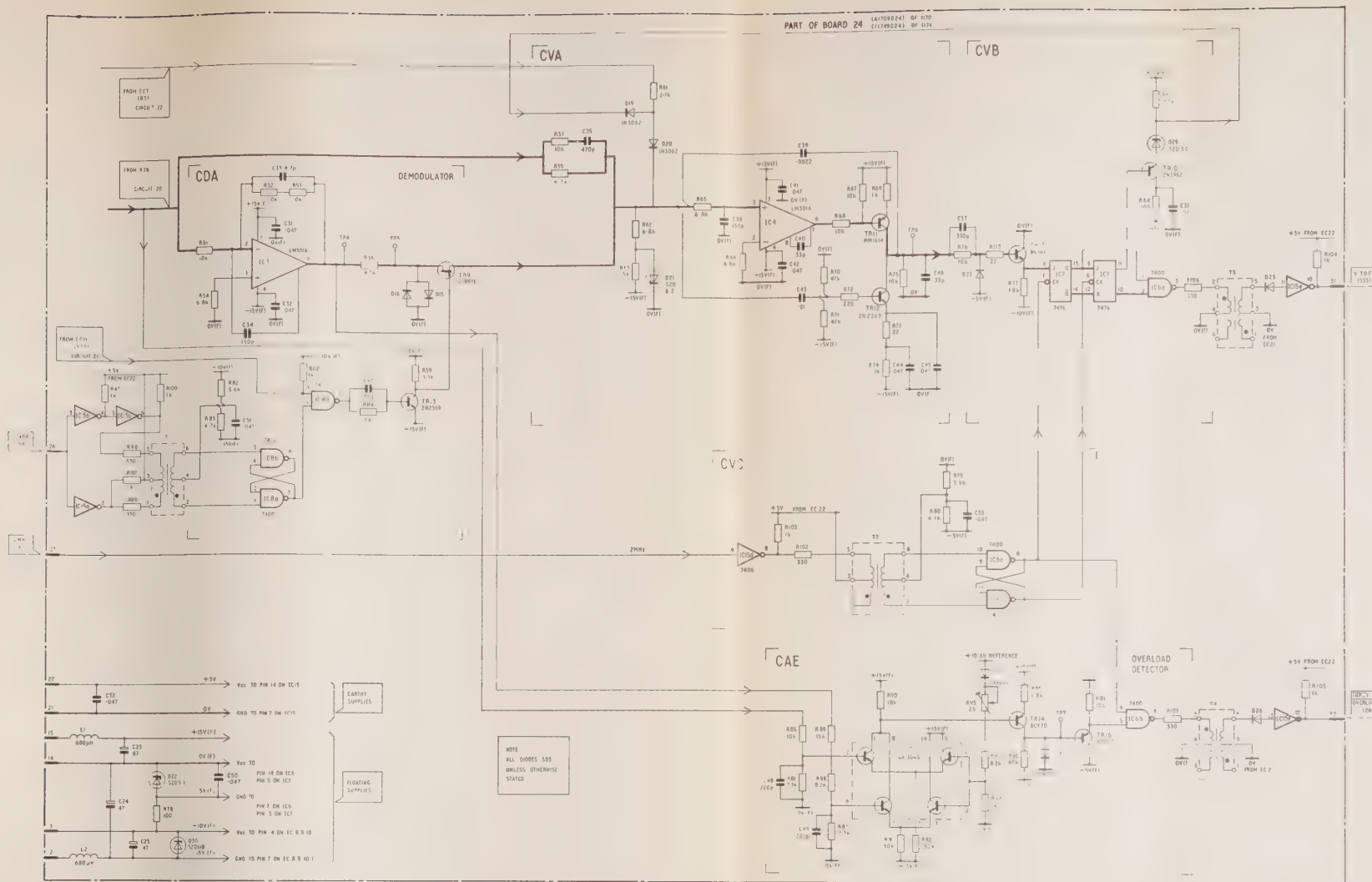
Circuit 21

The principle of the demodulator is shown in the block diagram for the input system. If Hetera-
dyne, demodulate or measure bias mode is in operation the connection from circuit 20 (573)
enables the chop input (66). This will chop the main signal at a frequency as explained in the block
diagram.

The V to f converter is also explained in the block diagram.

The input overload output is used to operate the autorange system as well as to indicate overload.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 21		
SOURCE	SIG No.	DESTINATION
2	611	25.50.54.58.65.66.69.70.72.
52	66	
20	573	
22	83	
	555	54
14	260	73



Circuit 22

This circuit generates an analogue dc voltage, used to back-off the bias, by means of a digital signal with a variable mark-to-space ratio. The input to IC7 is proportional to the mean level of the variable mark/space input (419/417). The output of IC7 ramps up when enabled by the reset logic, controlled from input (425/426). The ramp slope is proportional to the mark/space ratio.

After a certain time the sample command will be given from input (455/456). The sampled ramp voltage will be held on the output of IC6 and updated periodically.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 22		
SOURCE	SIG No.	DESTINATION
72	455	21
72	456	
72	425	
72	426	
72	414	
72	419	
	82	
	83	

Circuit 23

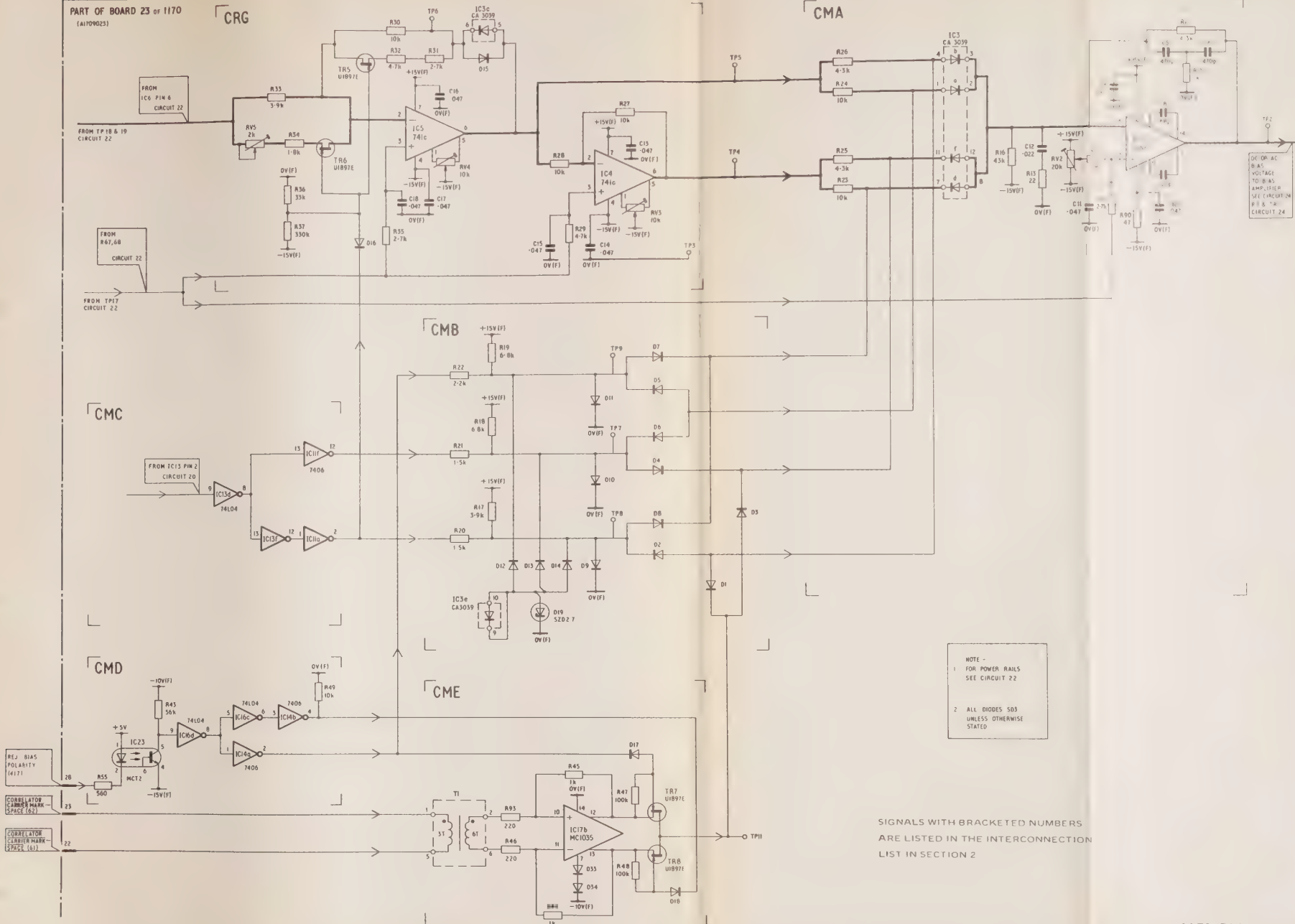
The dc voltage from circuit 22 is selected for polarity by block CMD from input (417). In the case of non-carrier mode this is a + or – decision.

If carrier mode is in operation demod will be called and blocks CME and CMC will be operative. In this case the mark/space representation of the carrier wave on inputs (61/62) will be used to modulate the voltage from circuit 22 in block CMA to provide an ac output at the carrier frequency. The phase will be determined by the bias reject decision in block CMD.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 23		
SOURCE	SIG No.	DESTINATION
69	61 62 417	

CRG

CMA



Circuit 24

The value of the bias reject voltage is determined by this selectable gain amplifier.

Interconnections		
Signal numbers are as in Section 2.4.		
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 24		
SOURCE	SIG No.	DESTINATION
63	50	
63	51	
	418	20
14	236	20

NOTE -
FOR POWER RANGES
SEE CIRCUIT 22

CBA

BIAS AMPLIFIER

FROM IC2
PIN 11
CIRCUIT 23

FROM TP2 ON DRG 23

REJECT BIAS
VOLTAGE (418)

CBB

BIAS RANGE
DECODE

DV FROM BOARD 24

REJECT
VOLTAGE (1236)

SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2

Circuit 25

The Strobe Generator (block FGA) generates a 0.5µs pulse at a prf of 500kHz. They are steered to each of 16 outputs in turn by IC25 and IC15, but only the outputs shown are used. Each output will receive 16 pulses in a complete sequence of 256 counted by the binary down counter (block FCC).

The outputs 16 to 128 are used in circuit 29 to serialise data.

Although the circuitry is as shown here for 1174, some of the touch key functions are not used.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 25		
SOURCE	SIG No.	DESTINATION
72	174	30
2	611	21.50.54.58.65.66.69.70.72



Circuit 26

CIRCUITS 26 to 28

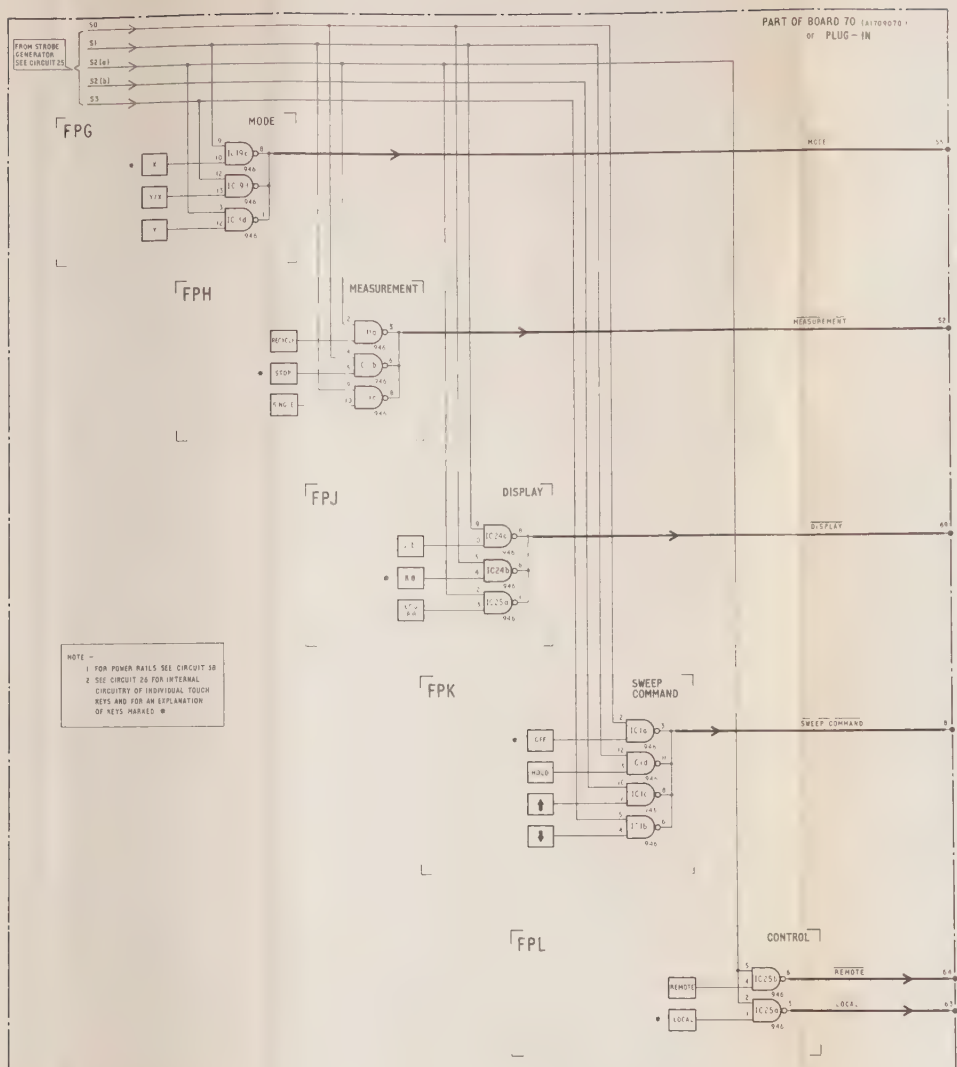
When a touch key is touched the output goes high. The appropriate output to circuit No. 29 will therefore go high during the particular strobe pulse.

Note that in the case of 1174 some of the touch keys are missing, although the circuitry is complete as shown here. These keys are those specifying the waveform, and the bias programming keys.

Circuit 27

CIRCUITS 26 to 28

When a touch key is touched the output goes high. The appropriate output to circuit No. 29 will therefore go high during the particular strobe pulse.

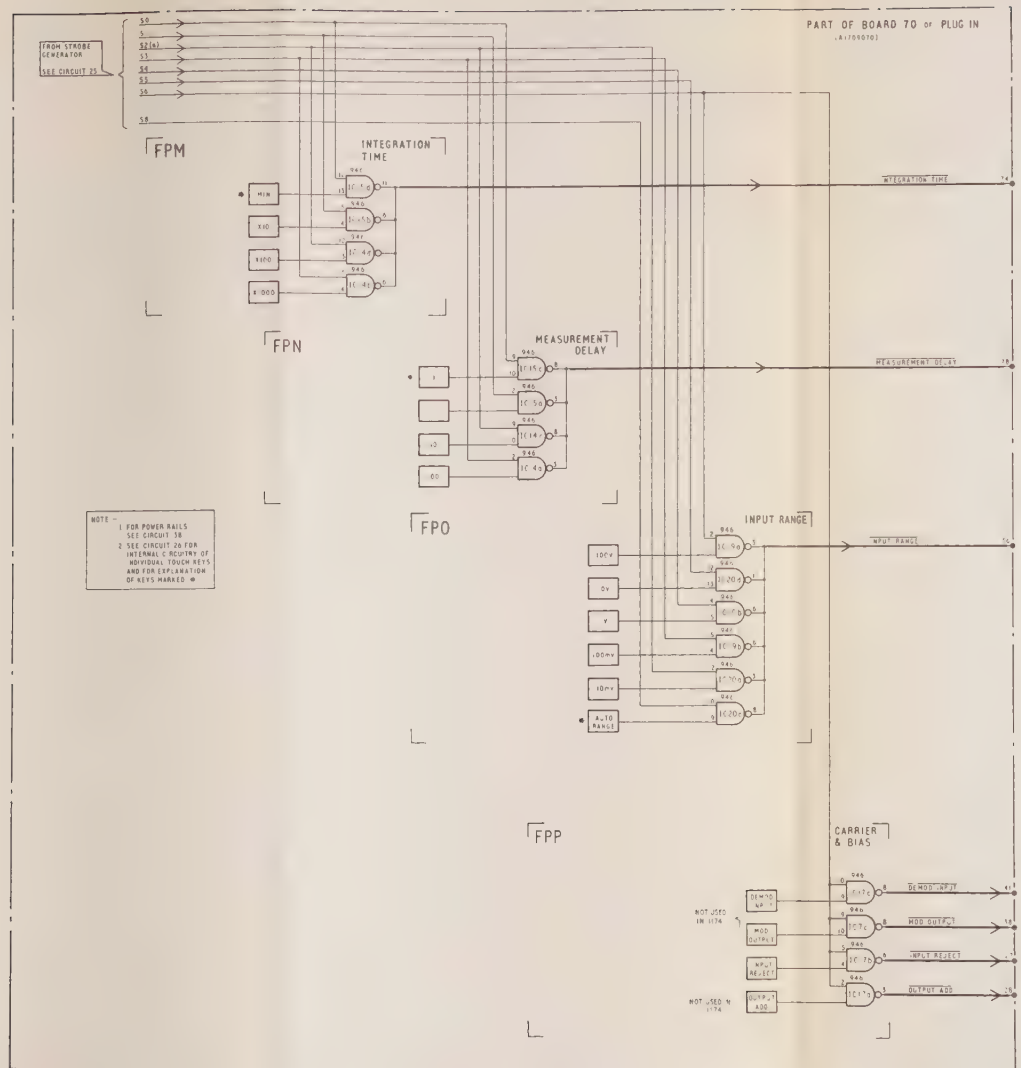


Circuit 28

CIRCUITS 26 to 28

When a touch key is touched the output goes high. The appropriate output to circuit No. 29 will therefore go high during the particular strobe pulse.

Note that in the case of 1174 some of the keys are missing, although the circuitry is complete as shown here. These keys are: Demod Input, Mod Output, and Output Add.



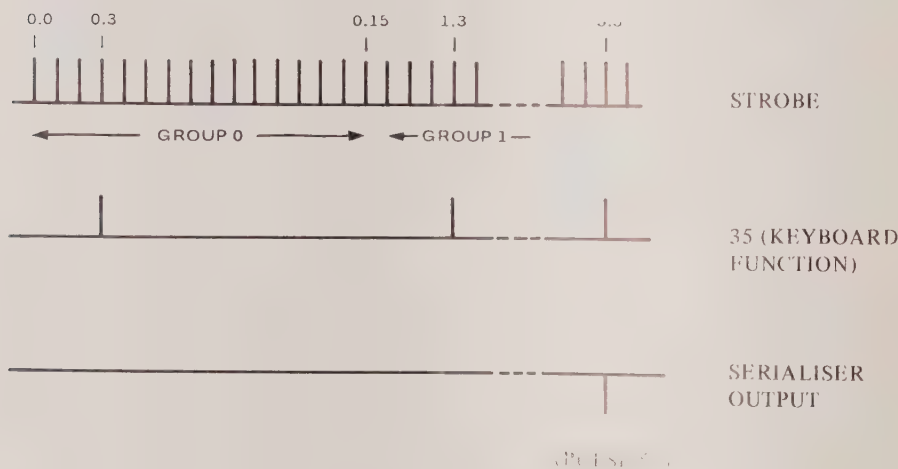
Circuit 29

Each output of circuits 25 - 28 is examined in turn by IC's 17 and 3. A particular touch key is identified by a low pulse at the output in one of 256 time slots of $2\mu s$. Note that not all of the touch key functions apply to 1174.

Example, See Figure Below

Consider that touch key Δf has been touched. The keyboard function (pin 35) line will go high for each strobe No. 3.

Each input to IC's 17 and 3 is examined for a period equal to 16 strobe pulses. The output will therefore go low for the period of strobe 3 of group 3. This is in fact the 52nd of the 256 time slots.



Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 29		
SOURCE	SIG No.	DESTINATION
62	438	33 73

Circuit 30

This circuit shapes the serial data for transmission to the 1170.

The click relay provides an audible indication that a front panel selection has been activated.

The mains set input sets all latch store data to a state equivalent to that required at power "switch-on".

Monostable IC5a ensures that once a serial data pulse has been detected any others are inhibited for its period.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 30		
SOURCE	SIG No.	DESTINATION
72	174	25
4	321	34.50.58.66
69	608	
	164	31

Circuit 31

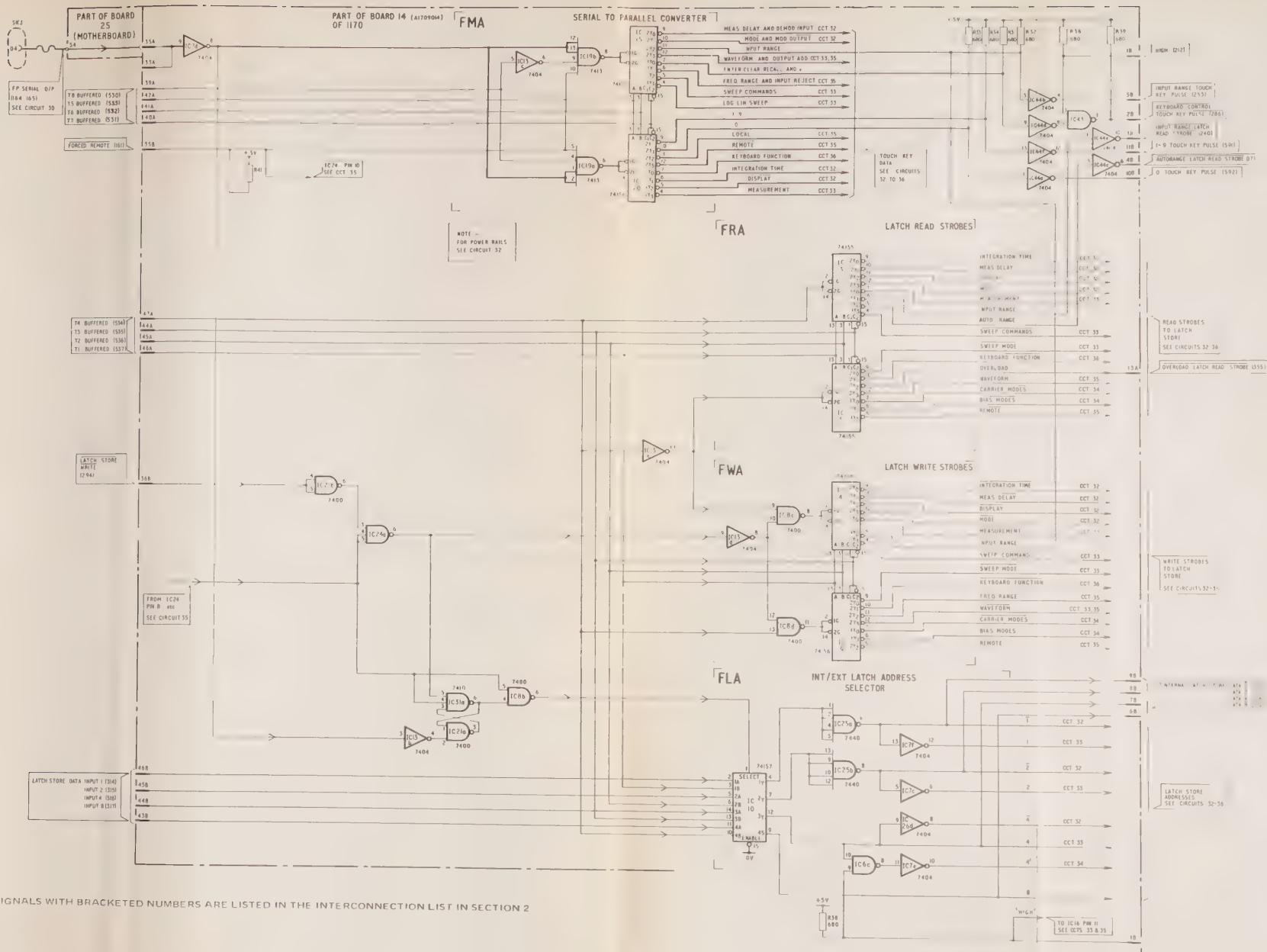
This circuit controls the writing-in and reading of data in the latch store (circuit 32 to 36). The same 256 bit timing sequence is carried on lines T1 to T8 (530 to 537) as is used in circuit 25. Note that some Latch Store functions are not used in 1174.

The 256 time slots are divided into 16 groups of 16. During each group, 16 Write and 16 Read strobes are generated at the same time as the data (from block FLA) increases in BCD from 0 to 15. Each output of block FMA is examined for the period of 1 group of 16 strobes. If a data pulse is received it will cause that particular output to change for the period of the particular time slot.

A particular bit of serial data will therefore coincide with a unique combination of outputs from blocks FMA, FWA and FLA, causing that particular bit to be written into the correct store location.

Numerical data from the keyboard are not stored in the Latch stores on pcb 14 but are passed directly into pcb 15 (circuit No. 70) via outputs (591/592). Autorange command is passed to pcb No. 17 (circuit No. 73). Input range data are held on IC30 on pcb No. 17 (circuit No. 73).

Interconnections		
Signal numbers are as in Section 2.4 Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 31		
SOURCE	SIG No.	DESTINATION
	317	
	316	
	315	
	314	
	294	
69	537	
69	536	
69	535	
69	534	
	161	35
69	531	
69	532	
69	533	
69	530	
30	164	
	165	
	212	36,70,71
	253	73
	286	70
	240	73
	591	70
	17	73
	592	70
	355	73
	256	36,70,71,73
	257	36,70,71
	258	36,70,71,73
	259	70,73



Circuit 32

CIRCUITS 32 to 36

The storage devices used to hold the front panel selections are "D" type flip flops.

Data are written - in by a clock pulse which is formed by a combination of a write strobe and a data pulse. The data that is written is generated in block FLA of circuit No. 31 (D inputs to the flip-flops).

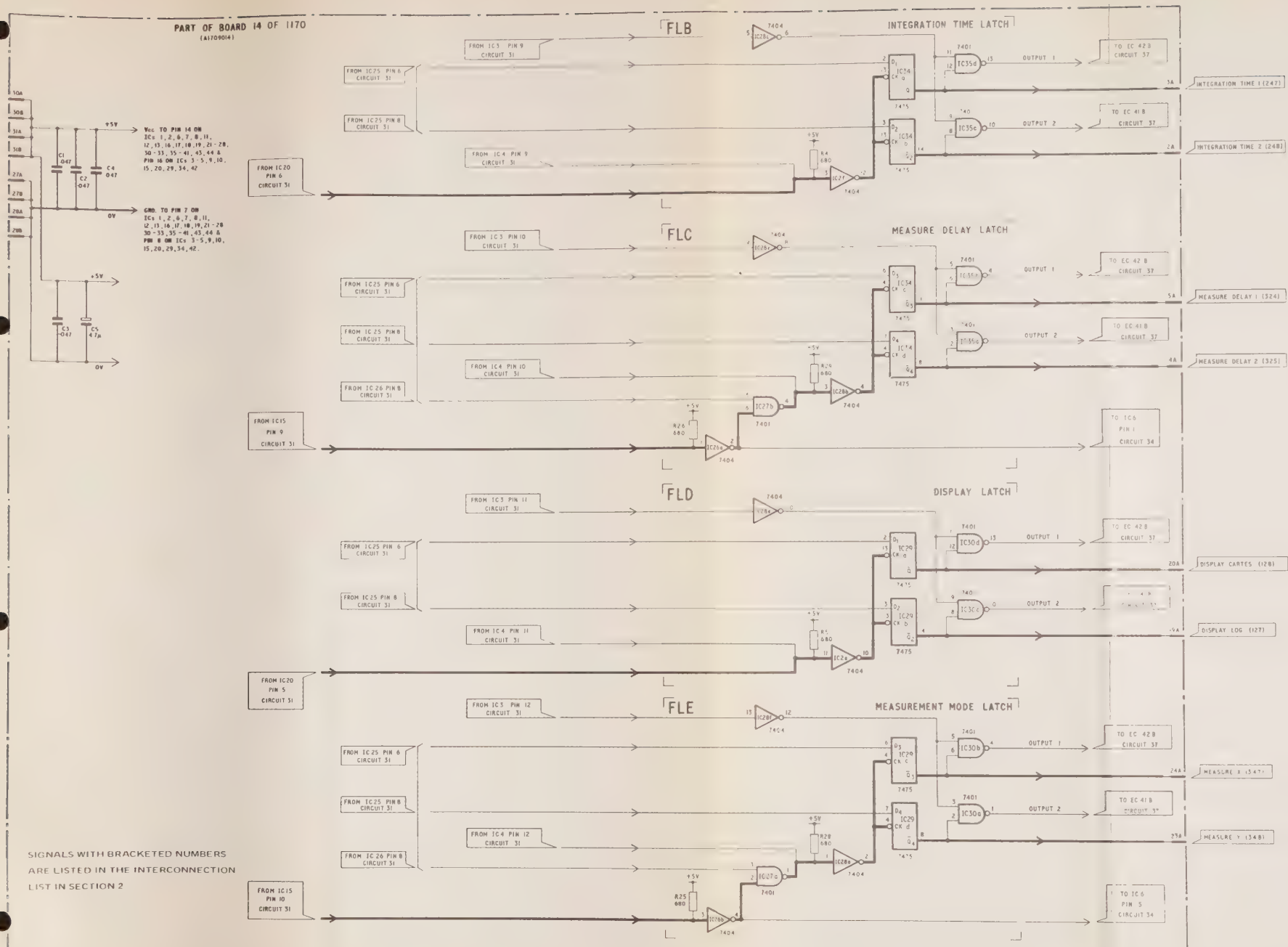
The store locations are best understood if the instructions for the use of the Store State Indicator are referred to. Table 2 of the SSI lists the Latch Store locations. The following table relates this information to the hardware.

Contents of the stores are read in sequence by the read strobes generated in block FRA of circuit 31.

Store Location	Function	Circuit No	Block	PCB	IC
0 - 0	Integration time	32	FLB	14	34
0 - 1	Measure delay	32	FLC	14	34
0 - 2	Display	32	FLD	14	29
0 - 3	Measurement	32	FLE	14	29
0 - 4	Measure Sequence	33	FLF	14	36
0 - 5	Input Range	73		17	30
0 - 6	Input Range	73		17	30
0 - 7	Sweep Command	33	FLG	14	32
1 - 0	Sweep Mode	33	FLH	14	39
1 - 1	Keyboard	36	FLO	16	36
1 - 2	Frequency Range	35	FLM	14	42
1 - 3	Generator Mode	35	FLL	14	42
1 - 4	Carrier Mode	34	FLJ	14	11
1 - 5	Bias Mode	34	FLK	14	22
1 - 6	Control	35	FLN	14	24

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 32		
SOURCE	SIG No.	DESTINATION
	247	50
	248	50
	324	50
	325	50
	128	69,71,74
	127	69,71
	347	64,69,71
	348	64,69,71

PART OF BOARD 14 OF 1170
(A1170014)



SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2

Circuit 33 See Circuit 32

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 33		
SOURCE	SIG No.	DESTINATION
62 62	486	
	438	29.73
	476	50.75
	415	64
	487	64
	122	73
	483	64
	484	64
	506	64.70
	313	36.71

PART OF BOARD 14 OF 1170
(L1170014)

FLF

MEASUREMENT LATCH

NOTE -
FOR POWER RAILS
SEE CIRCUIT 32

FROM IC3 PIN 7
CIRCUIT 31

FROM IC23 PIN 1
CIRCUIT 31

FROM IC25 PIN 8
CIRCUIT 31

FROM IC20
PIN 4
CIRCUIT 31

FROM IC4 PIN 4
CIRCUIT 31

FROM IC24
PIN 6
CIRCUIT 31

FROM IC14
PIN 8
CIRCUIT 31

FROM IC15
PIN 12
CIRCUIT 31

FROM IC10 PIN 12
CIRCUIT 31

FROM IC1 PIN 4
CIRCUIT 31

FLG

SWEEP COMMAND LATCH

FROM IC1 PIN 12
CIRCUIT 31

FROM IC1 PIN 8
CIRCUIT 31

FROM IC15
PIN 5
CIRCUIT 31

FROM IC4 PIN 4
CIRCUIT 31

FLH

SWEEP MODE LATCH

FROM IC15 PIN 8
CIRCUIT 31

FROM IC10
PIN 12
CIRCUIT 31

FROM IC15
PIN 4
CIRCUIT 31

FROM IC9 PIN 9
CIRCUIT 31

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

1170 LATCH STORE (2)

33

D11707033-02

Circuit 34 See Circuit 32

Note that some of the Latch Store functions do not apply to 1174 although the circuitry is complete as shown.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 34		
SOURCE	SIG No.	DESTINATION
4	321	30.50.58.66
	163	
	593	
	237	
74	125	20.52
	251	75
	337	41
	16	41
	416	64

Circuit 35 See Circuit 32

Interconnections		
Signal numbers are as in Section 2.4 Sources and destinations are circuit diagram numbers; if none shown all connections are within the circuit.		
CIRCUIT No. 35		
SOURCE	SIG No.	DESTINATION
	161	31
	173	71
	474	38
	497	38
	172	71
	171	71
	422	



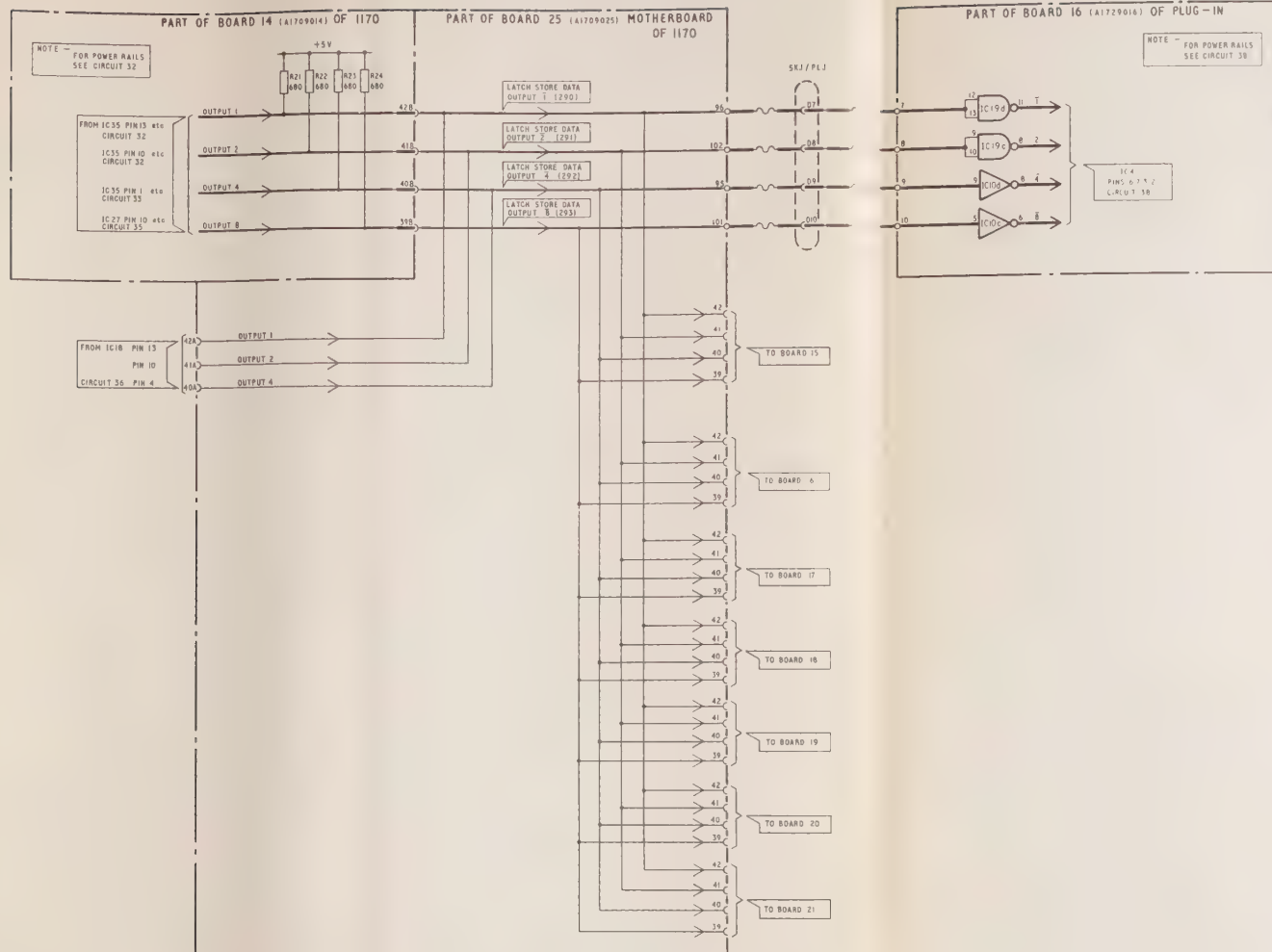
Circuit 36 See Circuit 32

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 36		
SOURCE	SIG No.	DESTINATION
31	258	70.71.73
31	257	70.71.73
31	256	70.71.73
31	212	70.71
33	313	71
71	485	70
71	274	70
71	275	70
71	276	70
71.73	290	37
71.73	291	37
71.73	292	37
	287	71
	288	71

Circuit 37

The Latch store outputs are connected together in this circuit to form the Latch Store Output Busses. The data held on these busses represents the contents of each store, in turn, in a 16 bit sequence at 500kHz.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 37		
SOURCE	SIG No.	DESTINATION
36.71.73	290	
36.71.73	291	
36.71.73	292	
73	293	



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 38

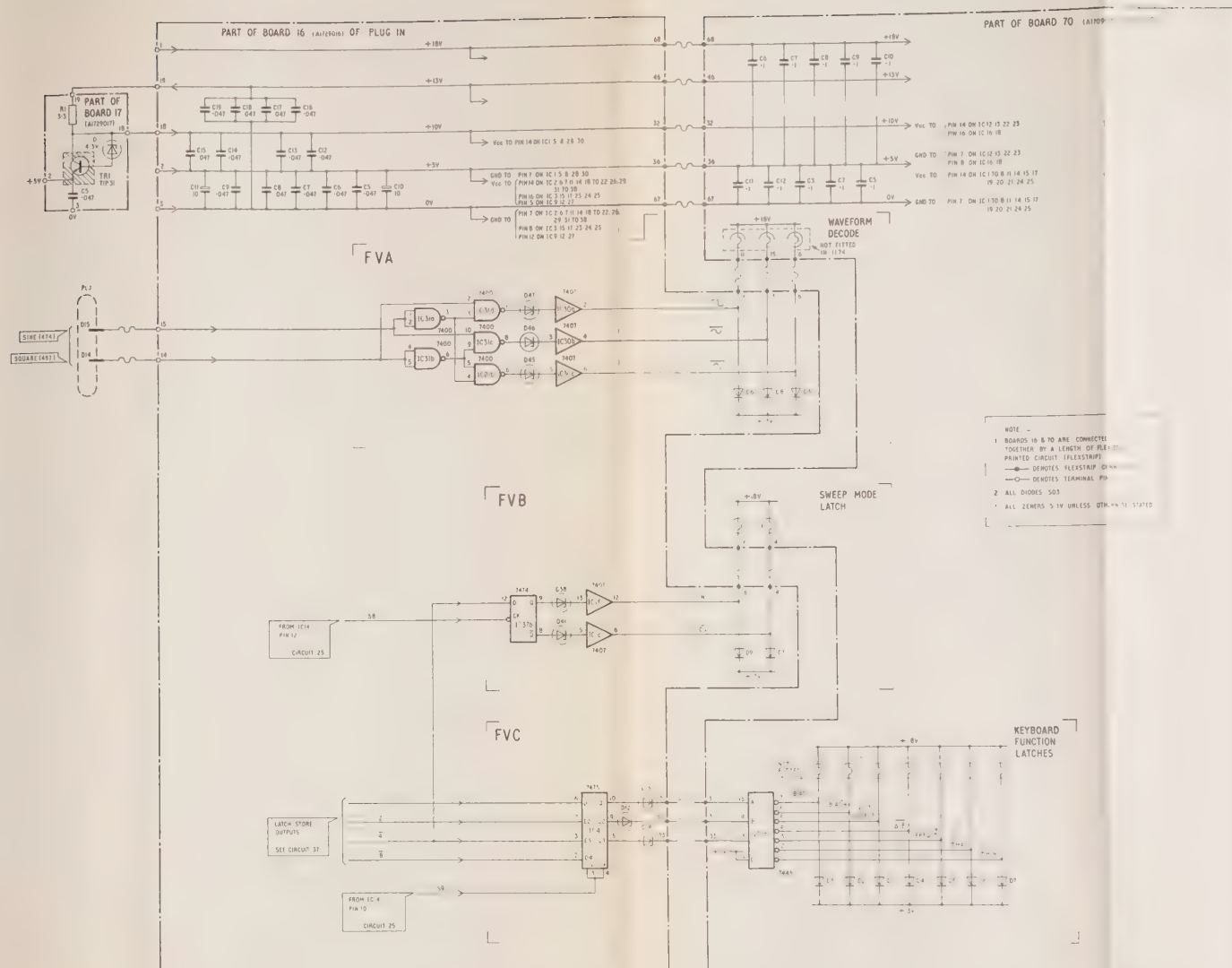
CIRCUITS 38 to 41

Each Touch Key Latch is strobed in turn from circuit No. 25. This causes the data held in the Latch Store to be copied into the latches on these circuits and the appropriate light to glow.

The generator Mode, Modulate, and Bias Add data are carried on single lines from the Latch Store and are not strobed as are the others. The Mode state is used elsewhere within the generator; the other two are not used within the 1174.

With the exception of the relevant bulbs for functions which are not used in the 1174, the touch key circuitry is as shown in these diagrams.

Interconnections		
Signal numbers are as in Section 2.4.		
Sources and destinations are circuit diagram numbers; if none shown all connections are within the circuit.		
CIRCUIT No. 38		
SOURCE	SIG No.	DESTINATION
35	497	
35	474	

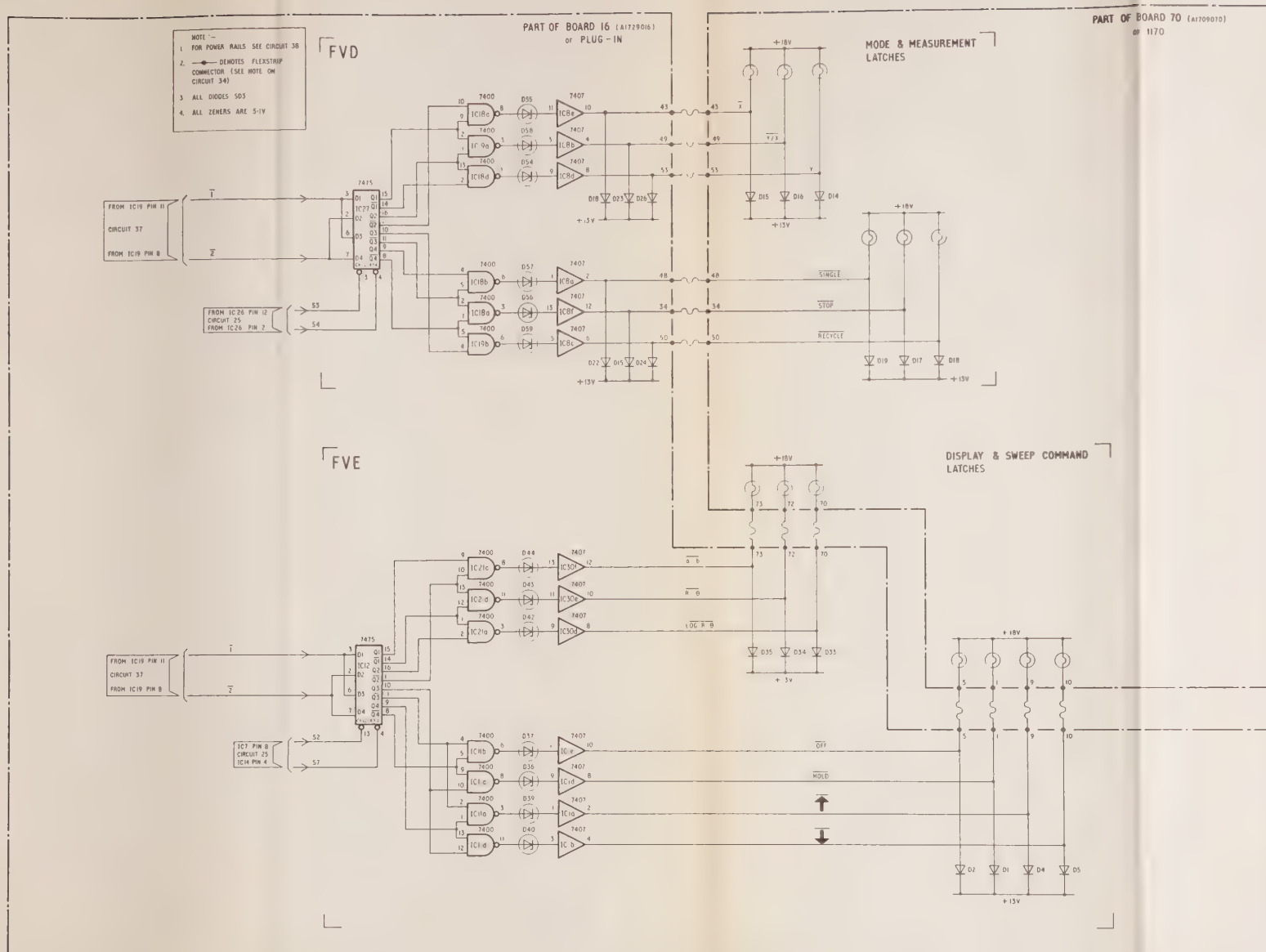


SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 39

CIRCUITS 38 to 41

Each Touch Key Latch is strobed in turn from circuit No. 25. This causes the data held in the Latch Store to be copied into the latches on these circuits and the appropriate light to glow.

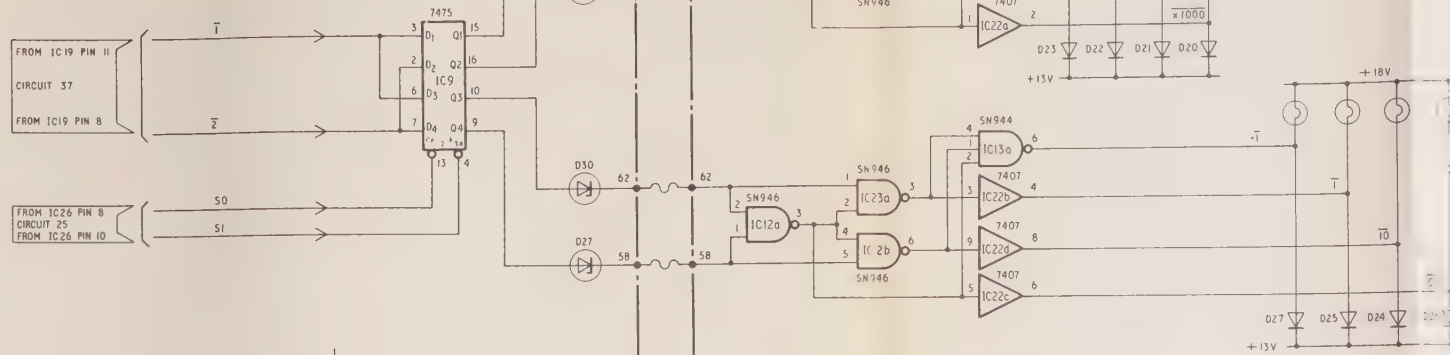


Circuit 40

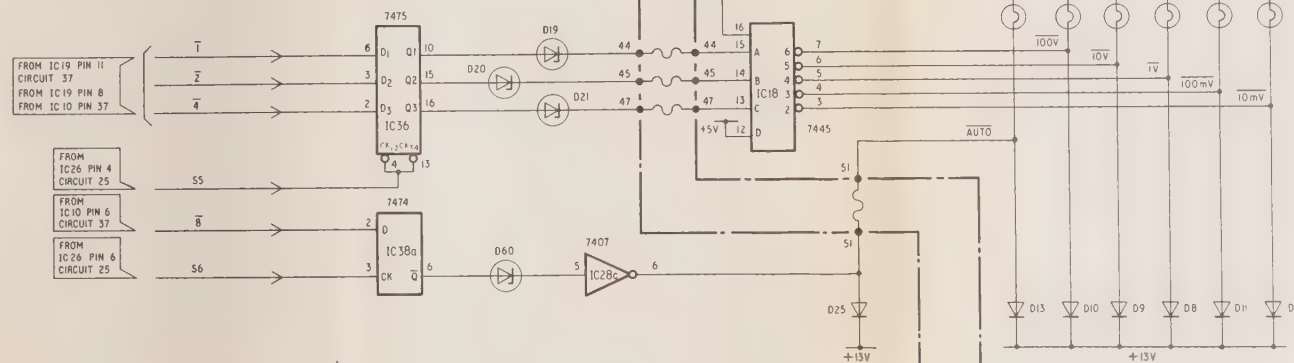
CIRCUITS 38 to 41

Each Touch Key Latch is strobed in turn from circuit No. 25. This causes the data held in the Latch Store to be copied into the latches on these circuits and the appropriate light to glow.

FVF

INTEGRATION TIME &
MEASUREMENT DELAY

FVG

INPUT RANGE &
AUTO RANGE
LATCHES

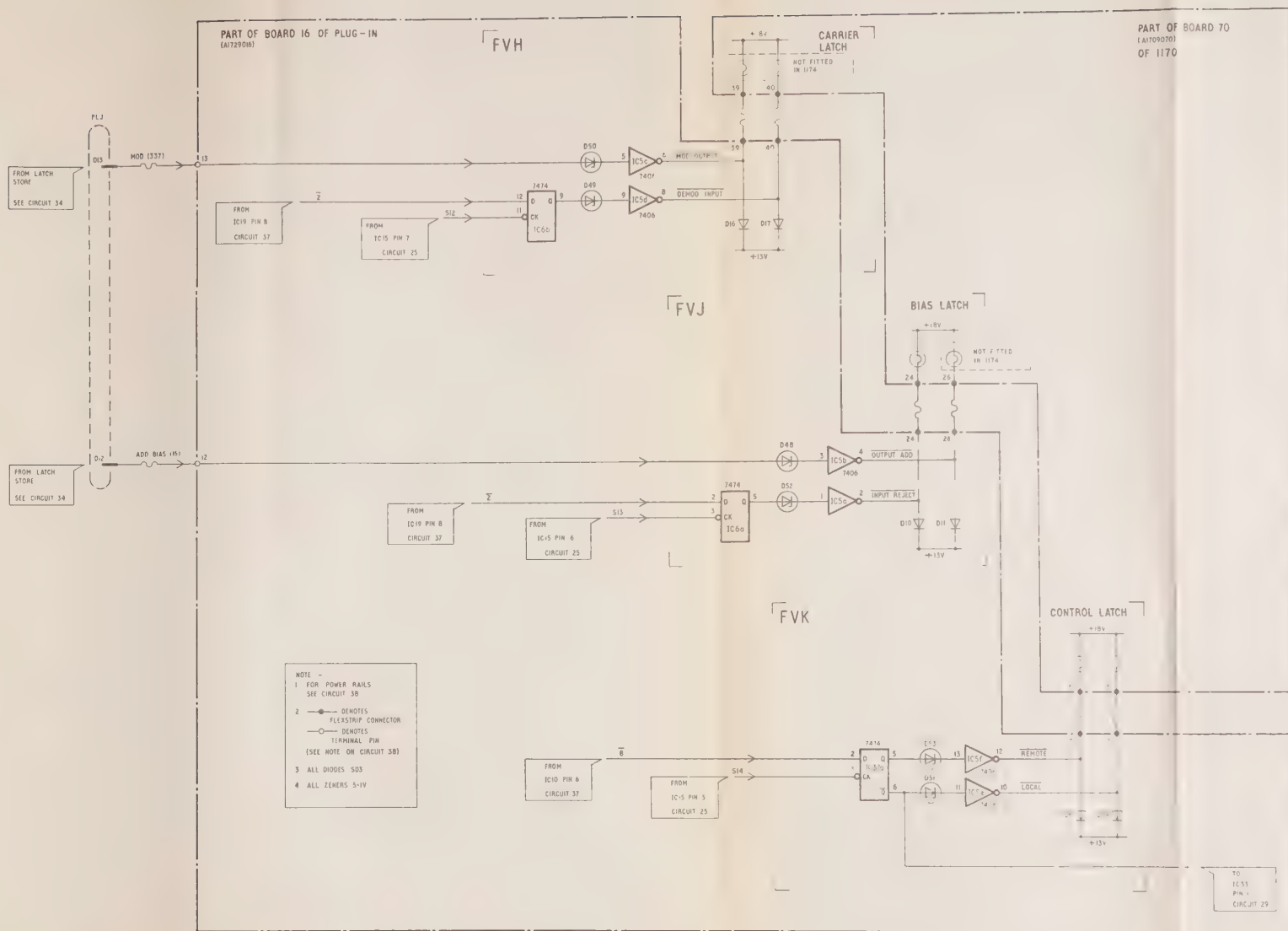
Circuit 41

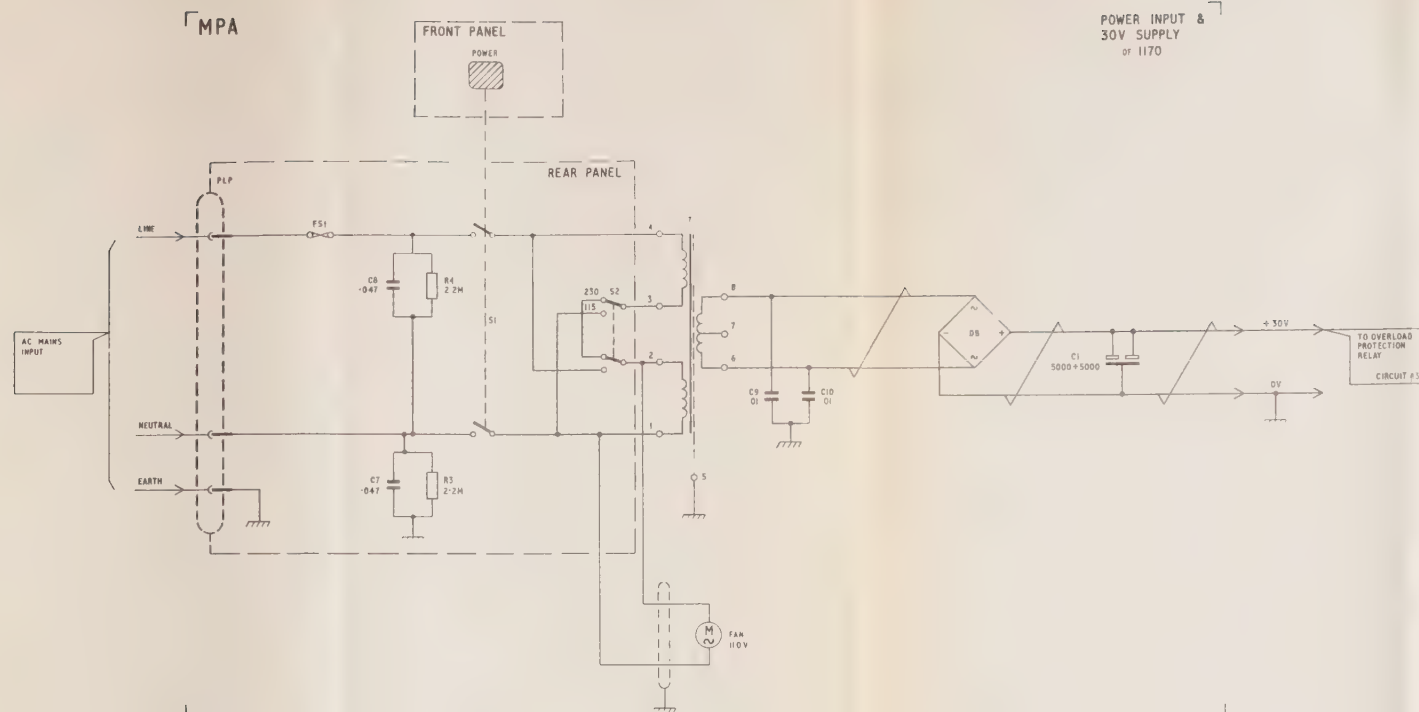
CIRCUITS 38 to 41

Each Touch Key Latch is strobed in turn from circuit No. 25. This causes the data held in the Latch Store to be copied into the latches on these circuits and the appropriate light to glow.

Although the circuitry is as shown here for 1174 (with the exception of the bulbs), some of the touch key functions are not used.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 41		
SOURCE	SIG No.	DESTINATION
34	16	
34	337	





POWER INPUT &
30V SUPPLY
OF 1170

Circuit 43

POWER SUPPLIES

Power is derived from the +30V rail. This voltage is dropped to +18V and +5V by the switching regulators. The regulating elements TR1 and TR2 (MJ3771) are switched at 25kHz, the mark to space ratio deciding the regulated voltage.

The +5V supply is split into four separate rails, one of them (D) having its own shunt regulator. The D rail supplies the plug in peripheral positions and therefore has a variable load.

The unsmoothed +5V supply, which has a large 25kHz component, is used to supply the primary of the +11V and +16V supply transformer.

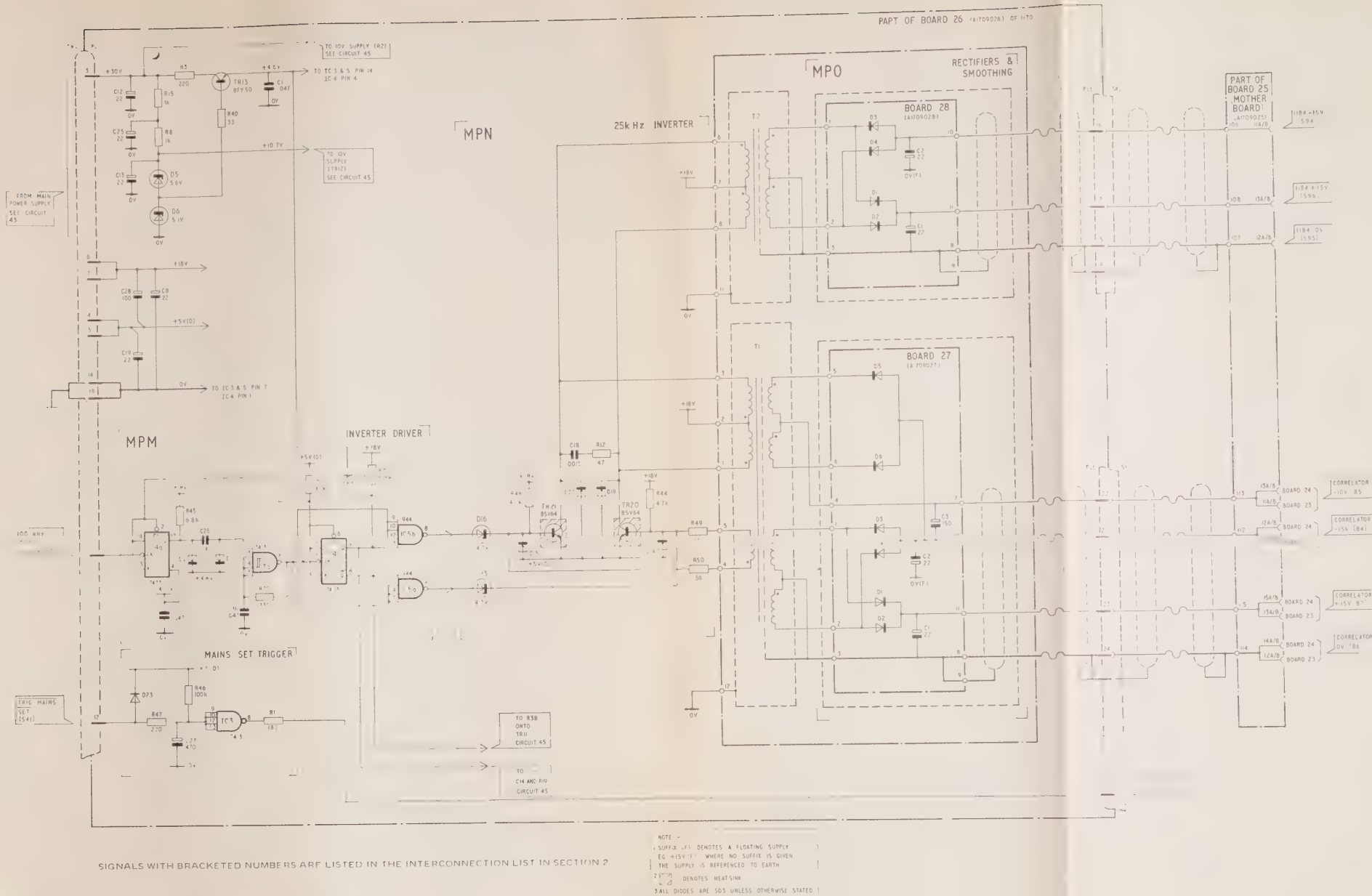
Each of the major rails has a series relay coil, the contacts of which are used to trip the +30V rail in the event of an overload ($> 6A$). In addition the +5V (D) rail will be overloaded, and so cause a trip, if an excess voltage is detected on the +18V rail.

Circuit 44

This circuit provides the necessary floating supplies for the input circuits (pcb's 23 and 24).

The 25kHz switching frequency used for the inverter and for the main switching regulators (circuits 45 and 43) is derived by dividing the 100kHz obtained from the plug-in.

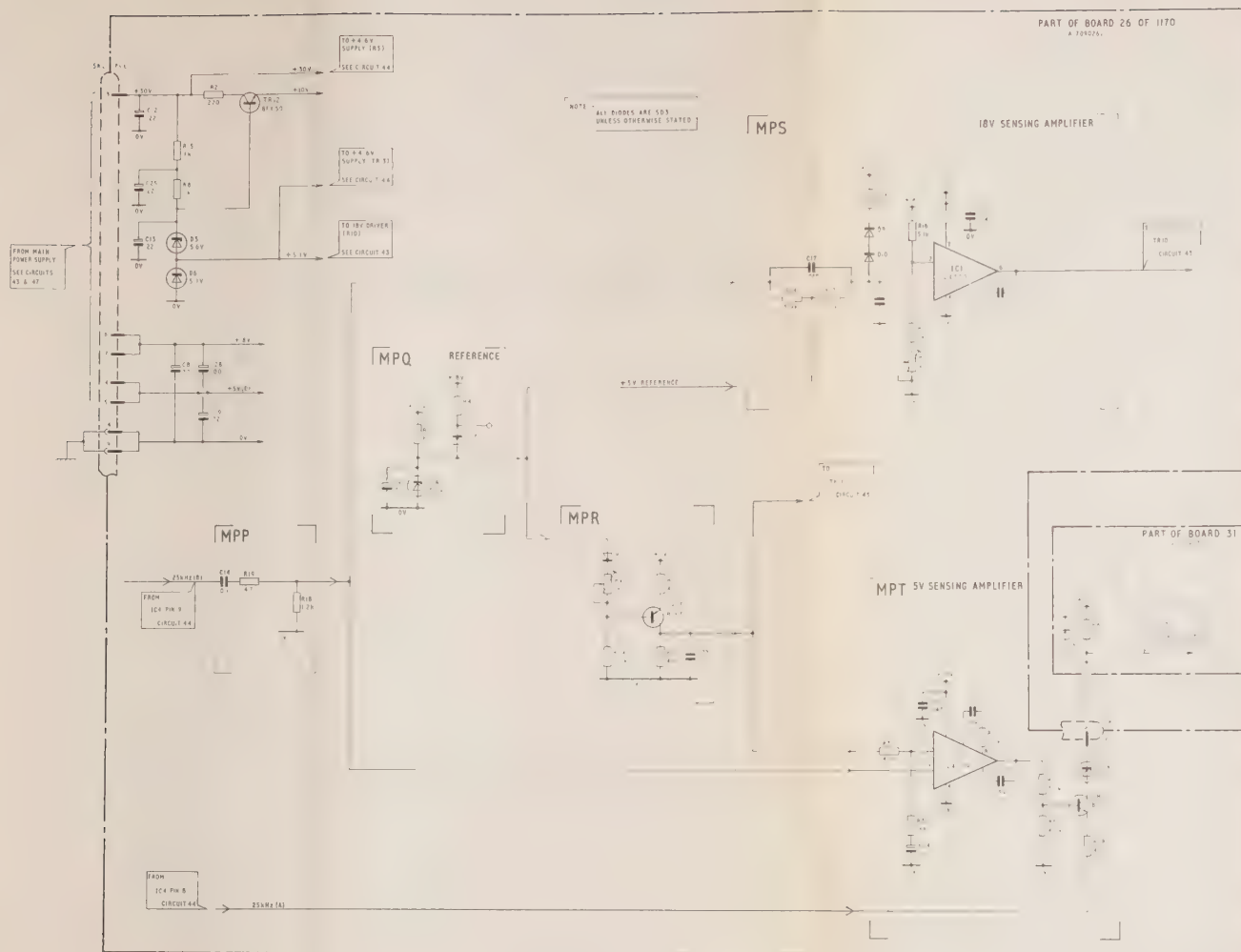
Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 44		
SOURCE	SIG No.	DESTINATION
68	541	5.54
2	606	
	594	
	596	
	595	
	85	
	84	
	87	4
	86	
	320	



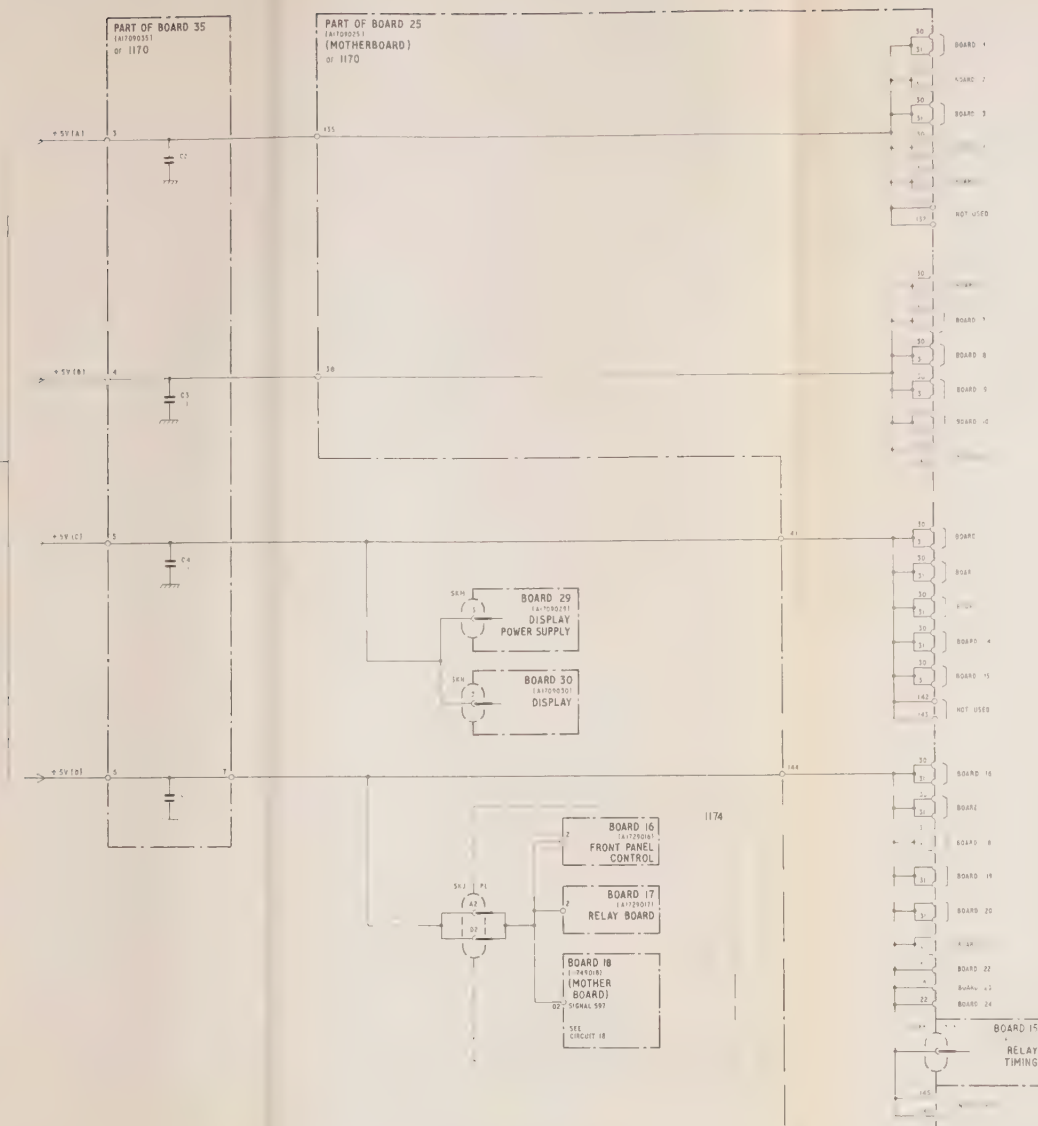
Circuit 45

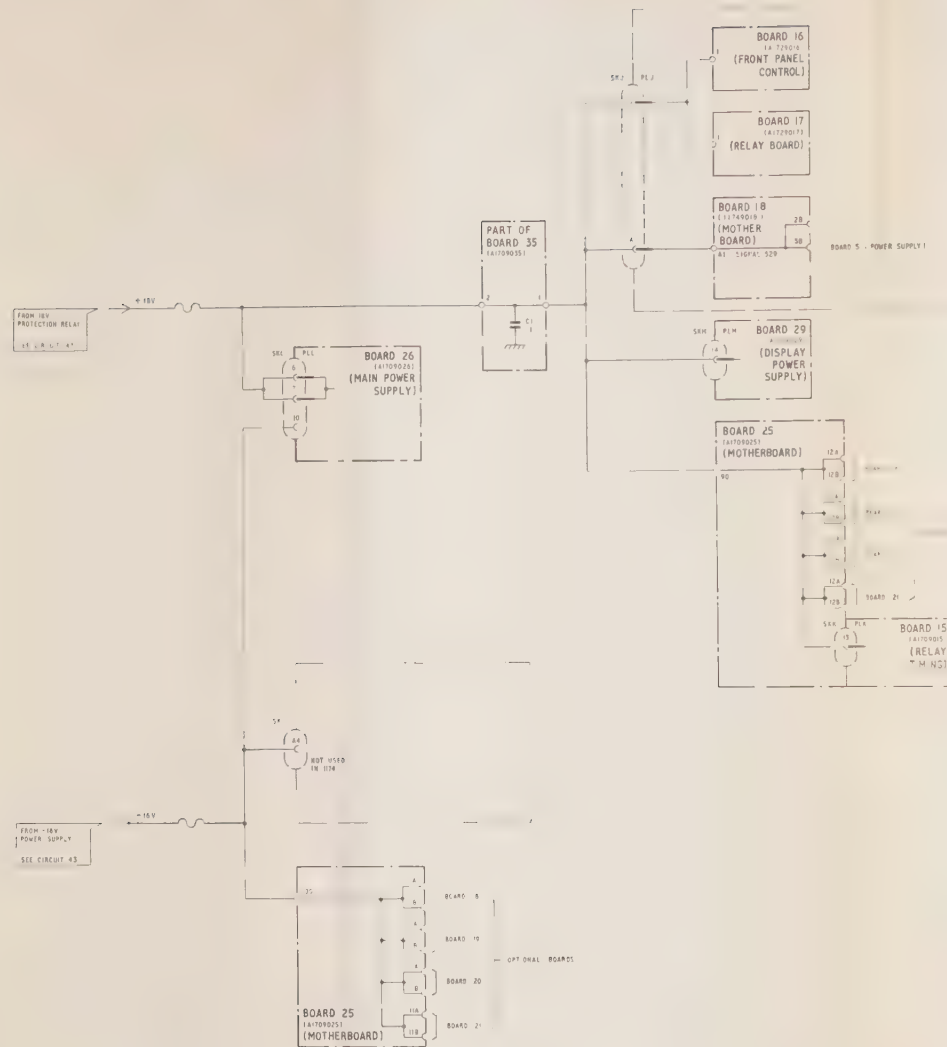
IC1 and IC2 have a 25kHz square wave input on terminal 3 and a variable dc input to terminal 2. The variable input is proportional to the sensed +18V or +5V rails. The outputs of IC's 1 and 2 are 25kHz square wave with mark to space ratios proportional to the +5V or +18V rails.

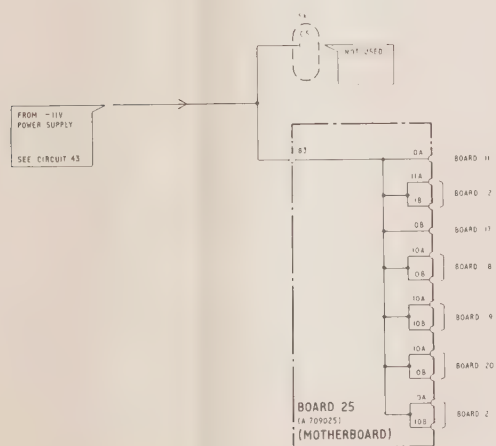
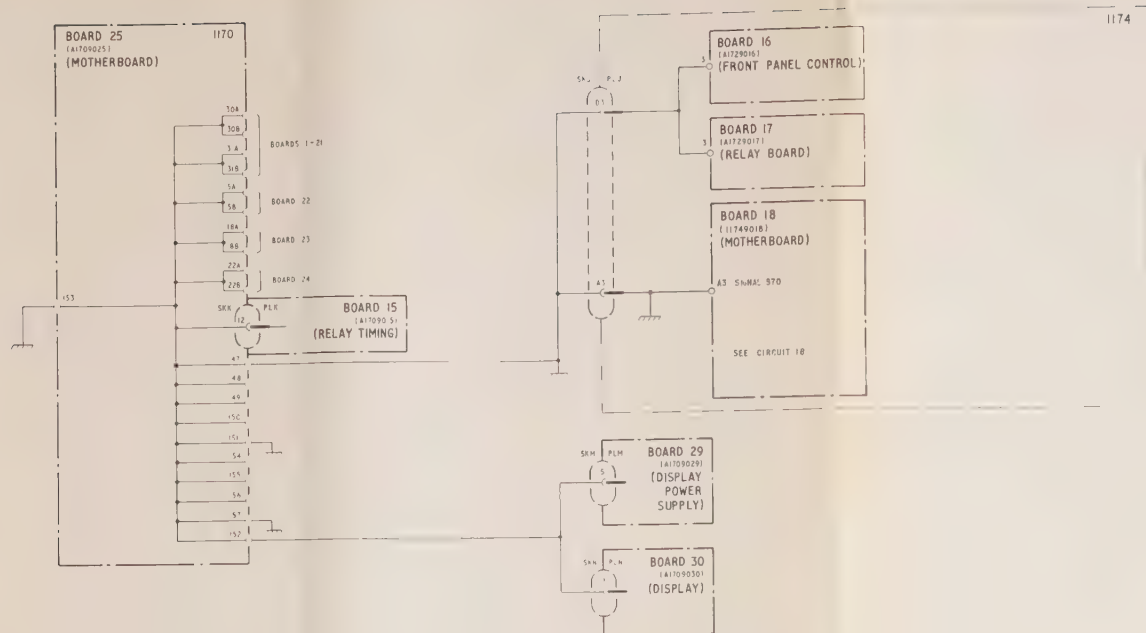
The output from block MPR to TR16 is a dc voltage proportional to the +5V (D) rail.



FROM 5V
PROTECTION
RELAYS
SEE FIGURE 43



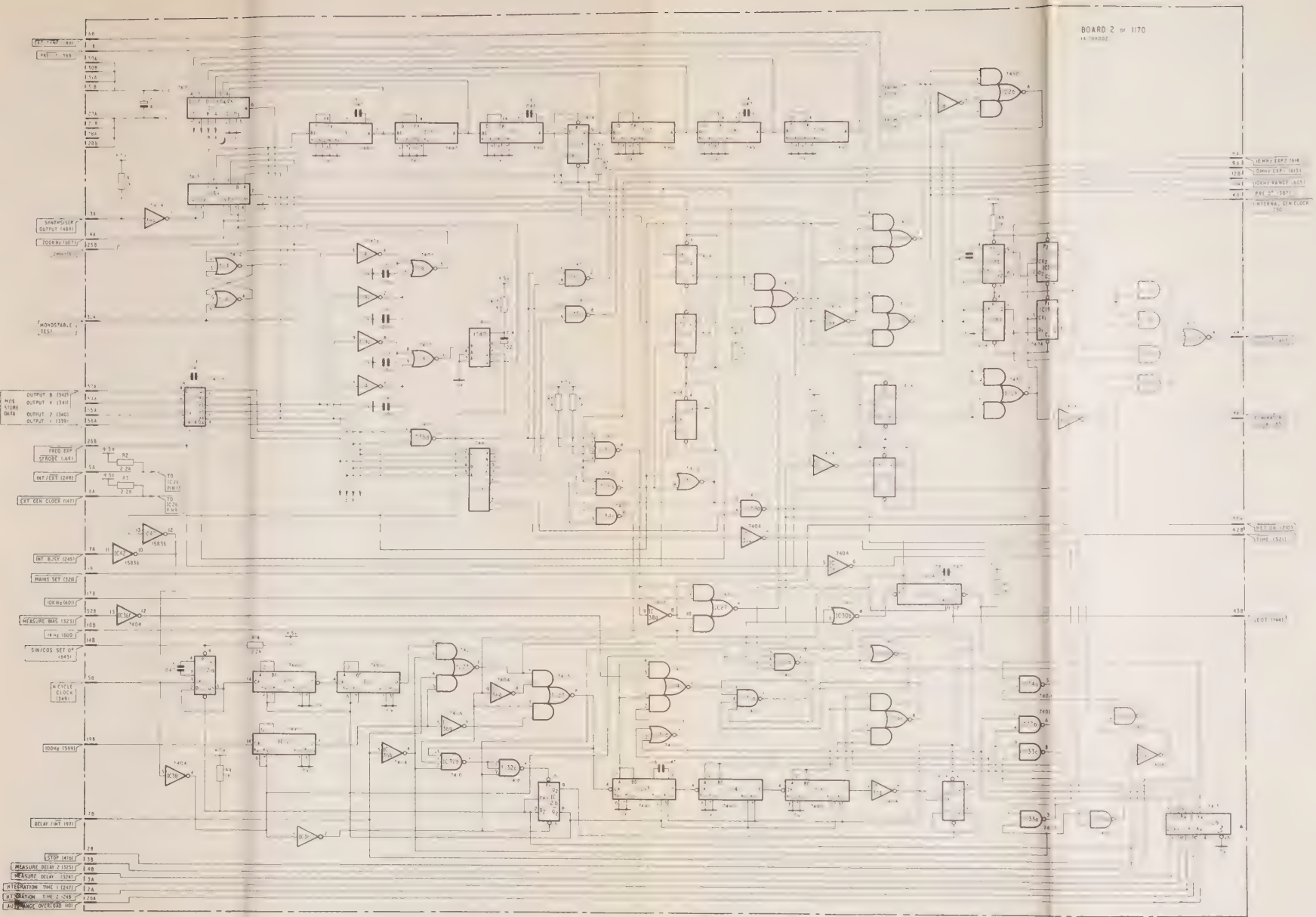




Circuit 50

This is one of the digital control circuits. A theoretical description is found in the description of the Arithmetic Unit

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 50		
SOURCE	SIG No.	DESTINATION
73	10	64
32	248	
32	247	
32	324	
32	325	75
33	476	
56	97	
2	599	1.14.54
52	349	12.54
52	645	
2	600	
62	323	20.52.56
2	601	12.54
4	321	30.34.58.66
54	245	3.63.69.70.71.72.74
	147	
	249	
69	169	3.63.70.71.72.74.
66	339	
66	340	3.63.70.71.72.73.74
66	341	
66	342	3.63.70.71.72.74
2	611	21.25.54.58.65.66.69.70.72
2	607	
11	489	9.10.11.12
1	388	
	149	
	614	
	613	11.12
	605	1
	387	12
	250	1.52
	463	
	185	
	210	
	521	54
	144	54



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

N CYCLE COUNTER AND
GENERATOR DIVIDER

Circuit 52

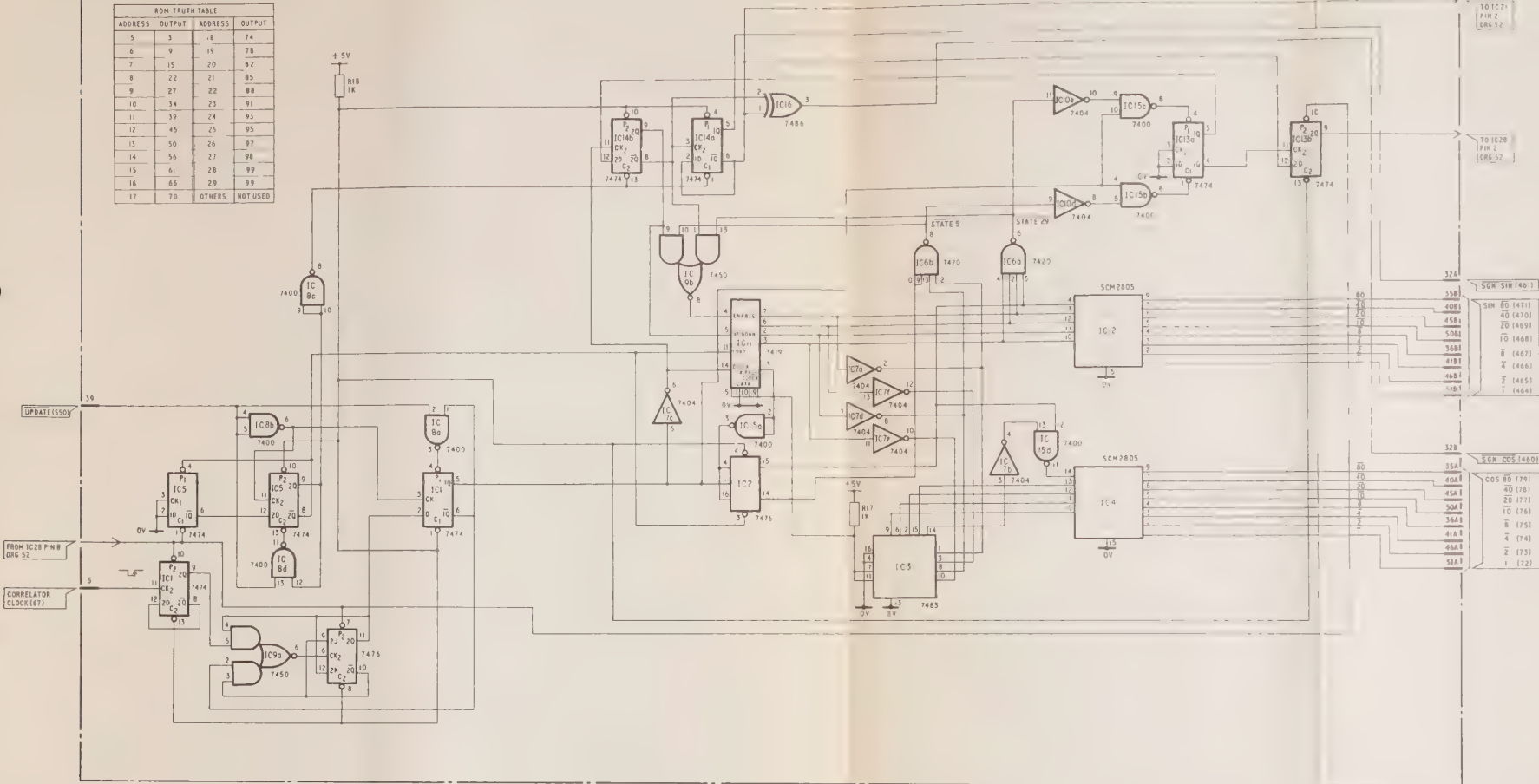
Interconnections		
Signal numbers are as in Section 2.4.		
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 52		
SOURCE	SIG No.	DESTINATION
	63	
34	125	20
62	323	20.50.56
50	210	20
	162	
50	387	
50	185	1
50	463	1
	645	50
	66	21
	67	53
	349	50



Circuit 53

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 53		
SOURCE	SIG No.	DESTINATION
54	67	52
	550	
55	461	55
	471	
55	470	
55	469	
55	468	
55	467	
55	466	
55	465	
55	464	
	460	55A
	79	55A
	78	55A
	77	55A
	76	55A
	75	55A
	74	55A
	73	55A
	72	55A

ROW TRUTH TABLE			
ADDRESS	OUTPUT	ADDRESS	OUTPUT
5	3	18	74
6	9	19	78
7	15	20	82
8	22	21	85
9	27	22	88
10	34	23	91
11	39	24	93
12	45	25	95
13	50	26	97
14	56	27	98
15	61	28	99
16	66	29	99
17	70	OTHERS	NOT USED



Circuit 54

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 54		
SOURCE	SIG No.	DESTINATION
57	544	
21	555	
2	611	21.25.50.58.65.66.69.70.72
2	599	1.14.50
2	600	12.50
2	601	12.50
2	606	5.44
2	609	
	550	53
56	335	
55	22	
56	494	
55A	23	
56	493	
50	144	
50	521	
56	244	55.57
56	590	
56	302	55.55A
2	616	
64	184	
55	309	
55	308	
55	310	
55	311	
64	120	56.57
64	119	56.57
64	118	56.57
	391	55.55A
	246	56
	361	55.55A
	52	56.57.64
	245	50
	336	55.55A
	80	55.55A
	331	55.55A
	254	56.57
	547	57
	459	55.55A

Alternative list for board 5
when fitted in position 6.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 55A			CIRCUIT No. 55A (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
54	336	55	53	75	
56	334		55	4	
56	332	55	55	37	
54	331	55	55	8	
54	361	55	53	78	
56	115	55	55	33	
61	136	56	53	74	
56	114	55		386	55.56
56	124	55	55	3	
56	478		55	36	
56	302	54.55	55	7	
54	80	55	53	77	
56	234	55	55	32	
55	385	56	53	73	
54	391	55	55	2	
56	11	55	55	35	
56	12	55	55	6	
56	64	55	53	76	
56	244	54.55.57	55	31	
53	460		53	72	
54	459	55	E	307	56.57.63.55
	117	56	E	306	56.57.63.55
	23	54	E	305	56.57.63.55
55	5		E	304	56.57.63.55
55	9				
53	79				
55	38				
55	34				

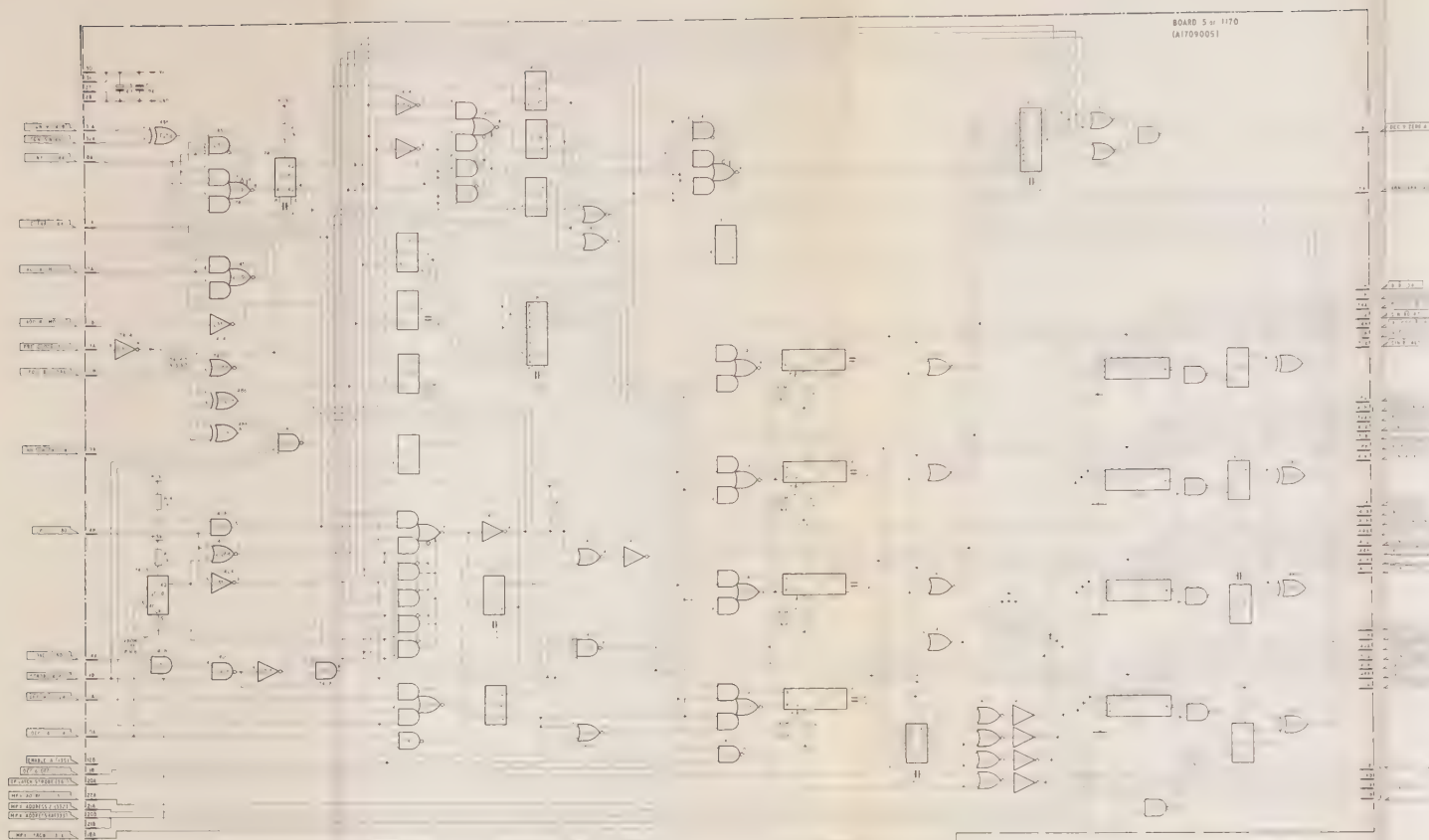
Circuit 55

This pcb is duplicated and fitted in position 5 and 6 of the 1170.

In some cases the use made of the edge connectors differs between the two positions.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 55			CIRCUIT No. 55 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
54	336	55A	53	5	55A
56	333		55A	467	
56	332	55A	54	33	
54	331	55A		310	
54	361	55A	55A	37	
56	115	55A	53	470	
61	135	56		8	55A
56	114	55A		4	55A
56	124	55A	53	466	
56	477			385	56.55A
56	302	54.55A	55A	32	
54	80	55A	54	309	
56	234	55A	55A	36	
55A	386	56	53	469	
54	391	55A		7	55A
56	12	55A		3	55A
56	11	55A	53	465	
56	64	55A	55A	31	
56	244	54.55.55A	54	308	
53	461		55A	35	
54	459	55A	53	468	
	116	56		6	55A
	22	54		2	55A
55A	34		53	464	
54	311		E	307	56.57.63.55A
55A	38		E	306	56.57.63.55A
53	471		F	305	56.57.63.55A
	9	55A	E	304	56.57.63.55A

← Alternative list for board 5 when fitted in position 6.



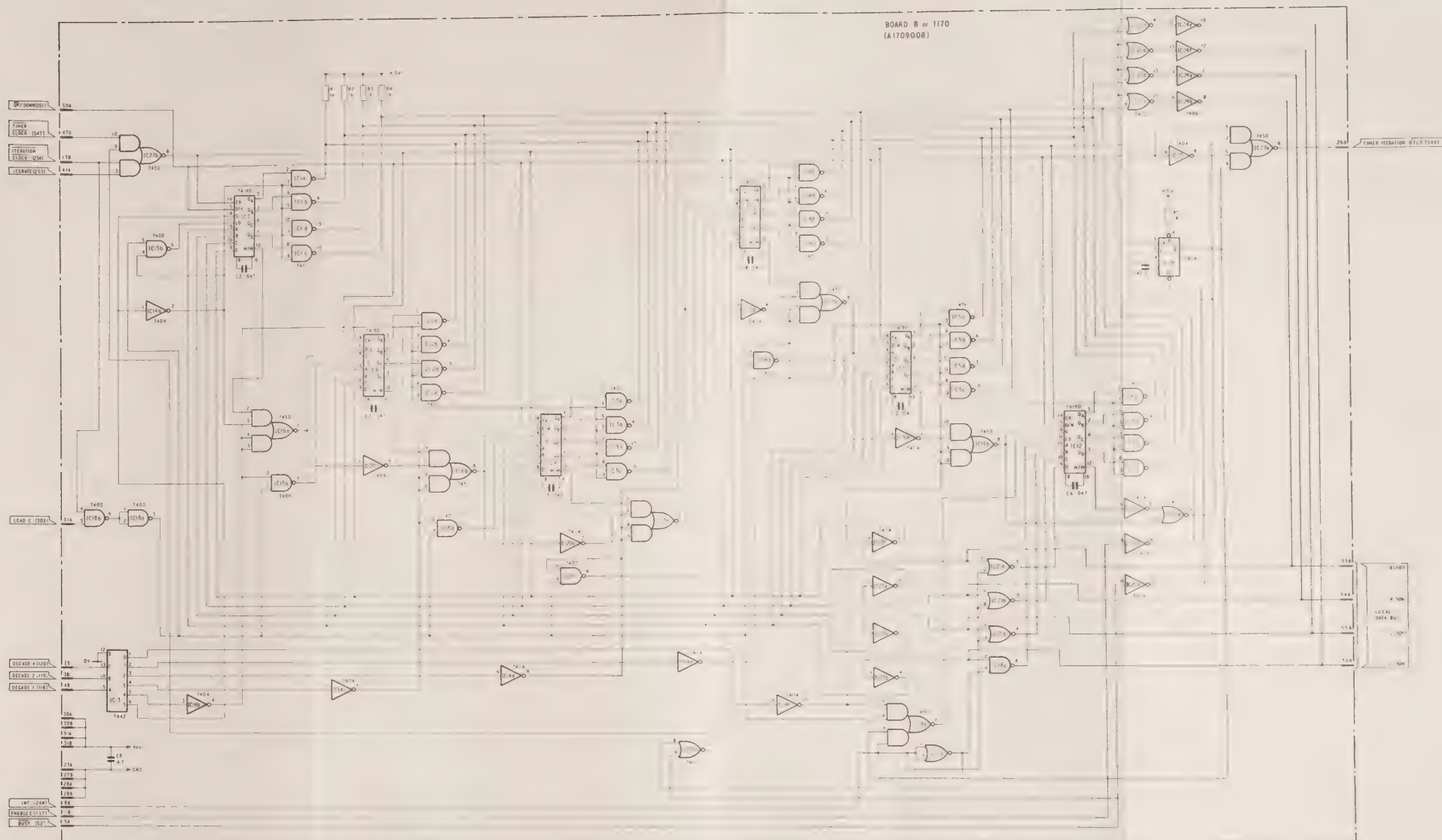
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 56

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 56			CIRCUIT No. 56 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
61	137	57		335	54
64	120	54.57		332	55.55A
64	119	54.57		333	55
64	118	54.57		334	55A
54	246			12	55.55A
	123			11	55.55A
54	254	57		551	57
	475			255	57
	160			590	54
62	323	20.50.52		64	55
73	312			302	54.55.55A
	488			493	54
63	408	58		494	54
54	52	57.64		478	55A
62	572			477	55
55A	386	55		234	55.55A
55	385	55A	E	304	55.57.63.55A
	148		E	305	55.57.63.55A
55A	117		E	306	55.57.63.55A
55	116		E	307	55.57.63.55A
62	81			244	54.55.57.55A
63	407	58		97	50
63	405	58.62		303	57
63	404	58		1	
63	403	58		30	
63	402	58		19	64
61	135	55.55A		20	64
61	136	55A		124	55.55A
				115	55.55A
				114	55.55A

Circuit 57

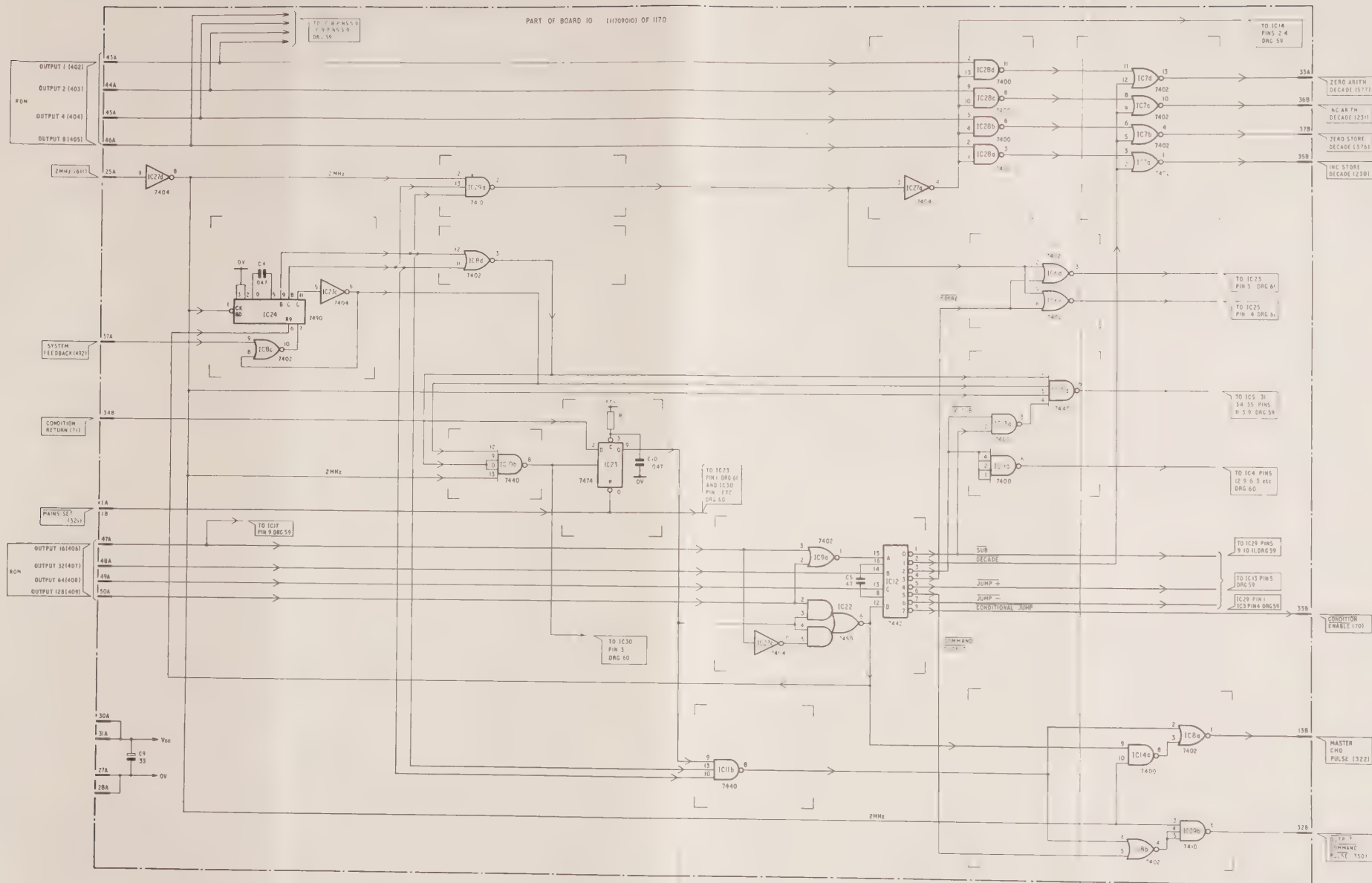
Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 57		
SOURCE	SIG No.	DESTINATION
54	52	56.64
61	137	56
56	244	54.55.55A
64	118	54.56
64	119	54.56
64	120	54.56
56	303	
56	255	
54	254	56
54	547	
56	551	
	544	54
	307	55.56.63
	306	55.56.63
	305	55.56.63
	304	55.56.63



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 58

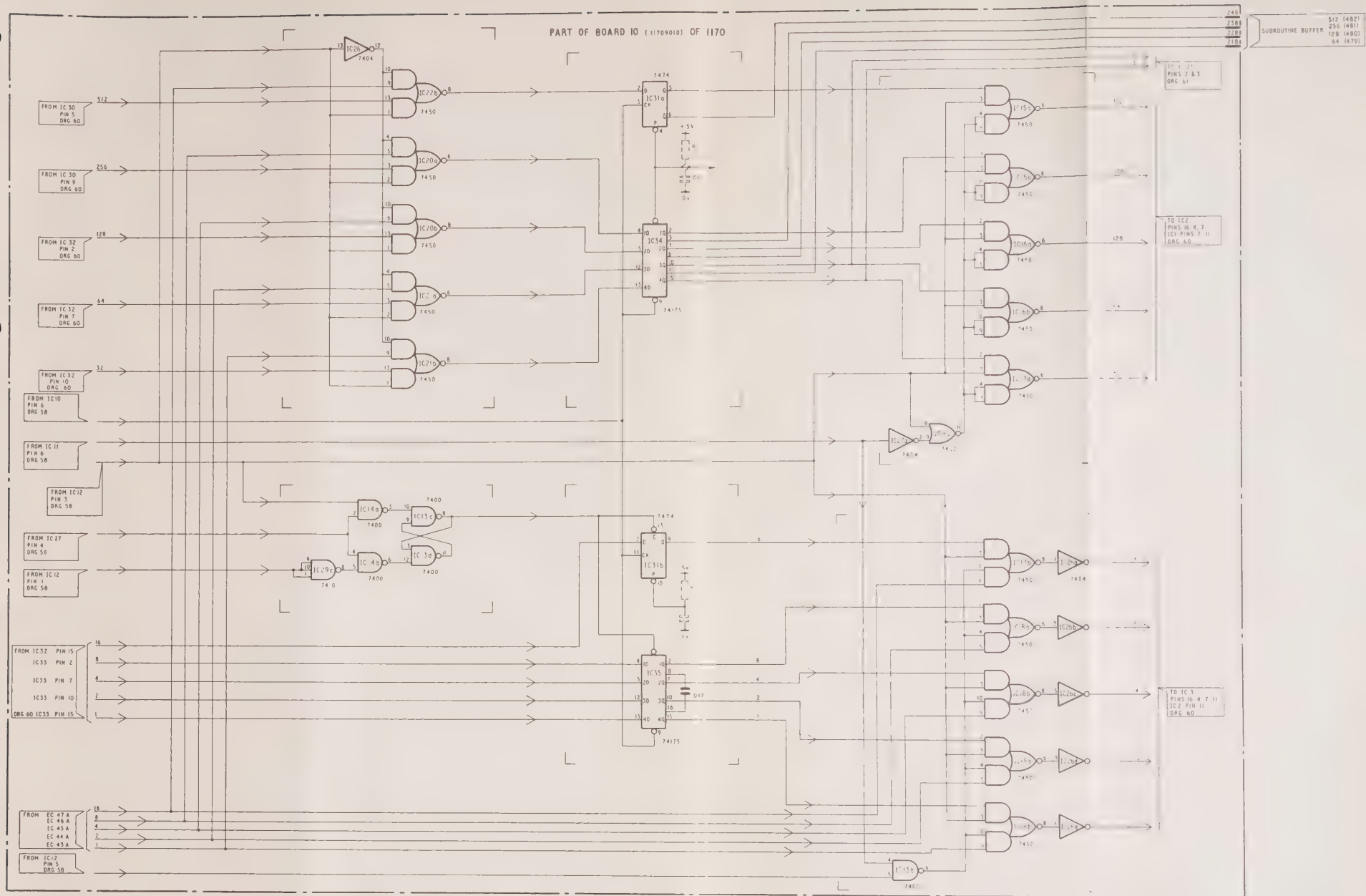
Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 58		
SOURCE	SIG No.	DESTINATION
63	409	
63	408	56
63	407	56
63	406	
4	321	30.34.50.66
64	71	
64	492	
2	611	21.25.50.54.65.66.69.70.72.
63	405	56.62
63	404	56
63	403	56
63	402	56
	577	64
	231	64
	576	65
	230	65
	70	64
	322	64
	350	62



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 59

Interconnections Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 59		
SOURCE	SIG No.	DESTINATION
	482	65
	481	65
	480	65
	479	65



Circuit 60

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 60		
SOURCE	SIG No.	DESTINATION
	428	63
	429	63
	430	63
	431	63
	432	63
	433	63
	434	63
	435	63
	436	63
	437	63

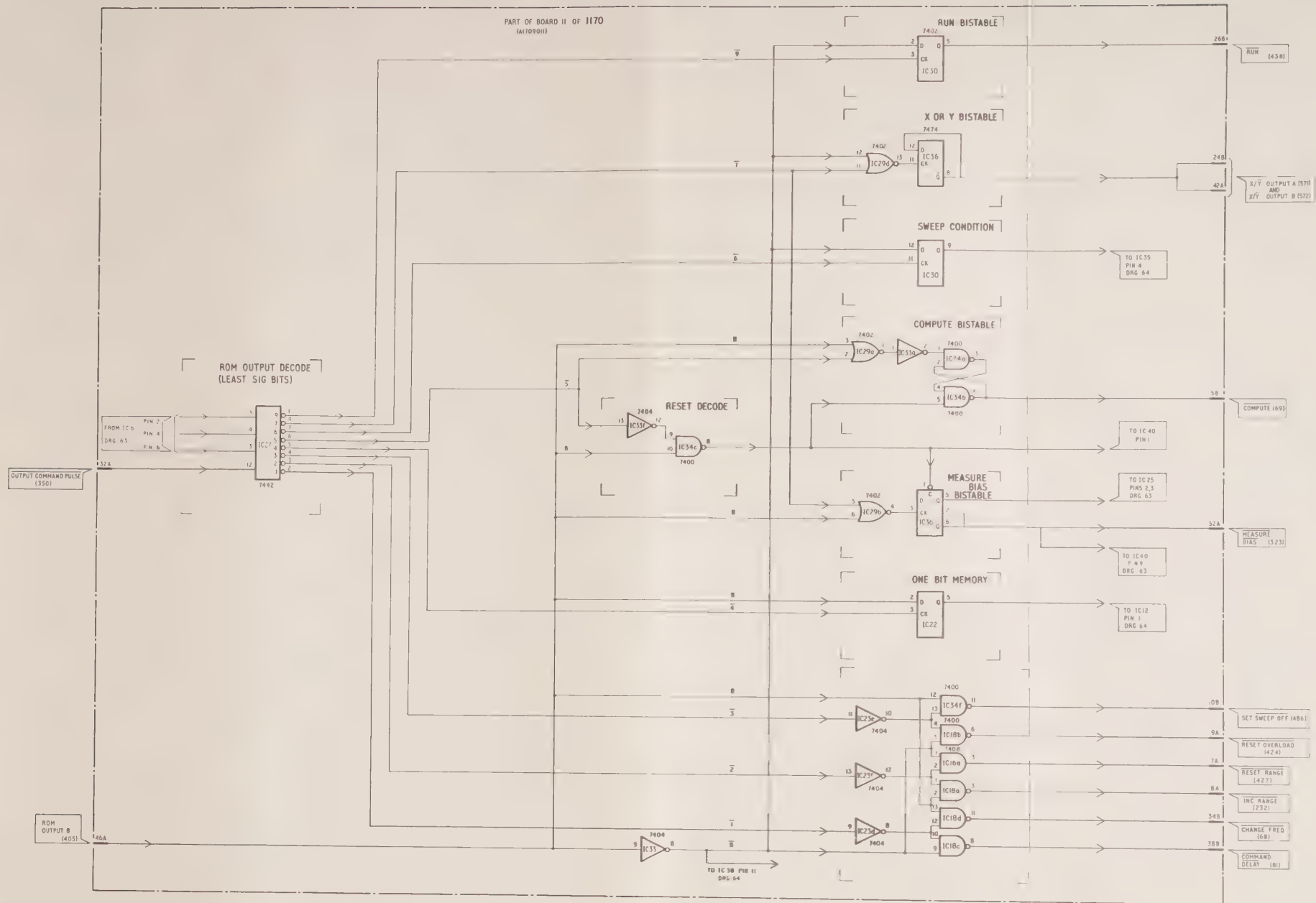
Circuit 61

Interconnections Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 61		
SOURCE	SIG No.	DESTINATION
	491	65
	138	64
	135	55.56.55A
	136	56.55A
	137	56.57
	495	65
	496	65

Circuit 62

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 62		
SOURCE	SIG No.	DESTINATION
63 58	405	56.58
	350	
	438	29.33.73
	571	1.14
	69	71
	323	20.50.52.56
	486	33
	424	73
	427	73
	232	73
	68	70
	81	56

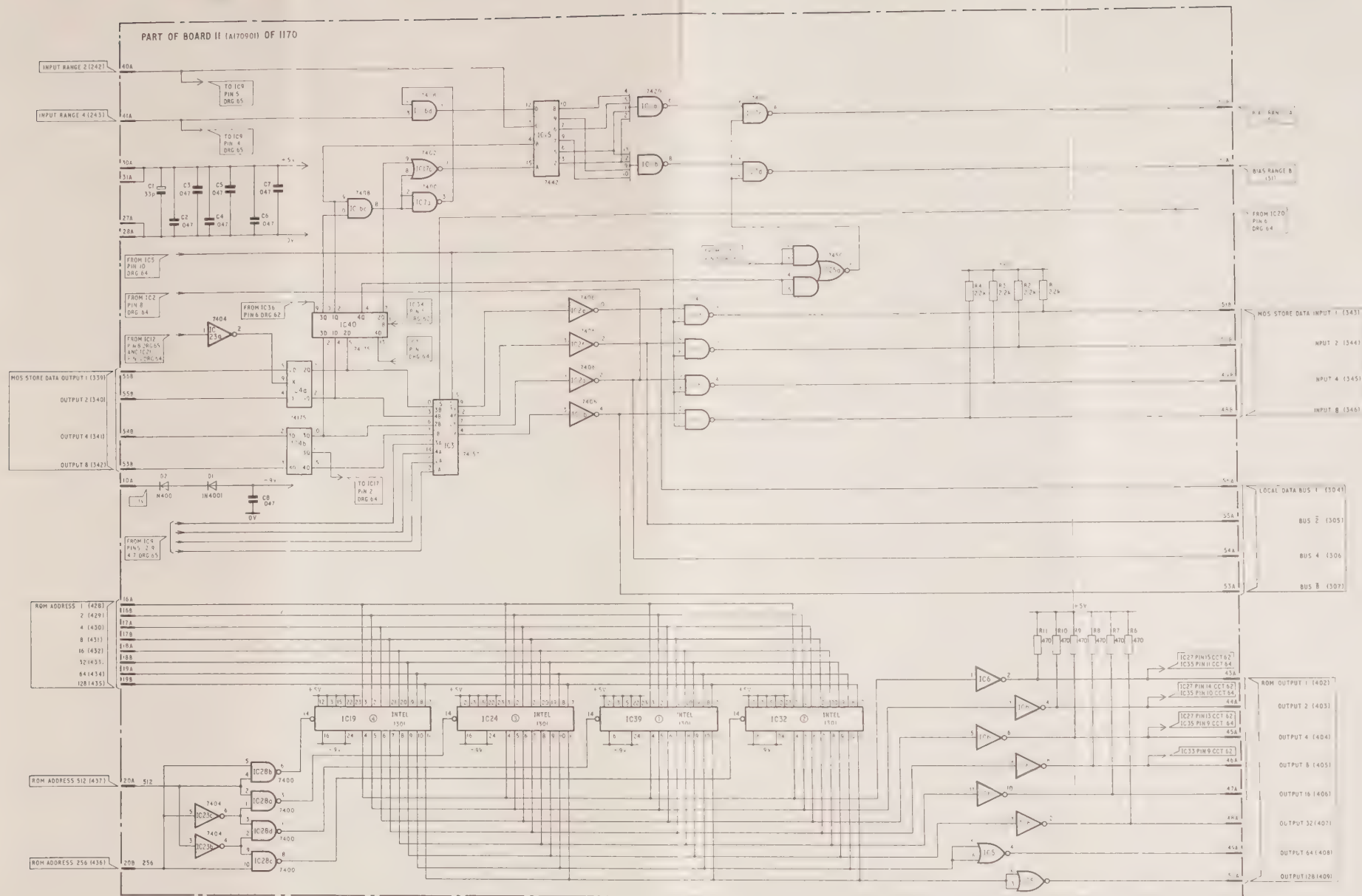
PART OF BOARD H OF 1170
(A1170901)



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

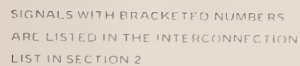
Circuit 63

Interconnections		
Signal numbers are as in Section 2.4.		
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 63		
SOURCE	SIG No.	DESTINATION
60	436	
60	437	
60	435	
60	434	
60	433	
60	432	
60	431	
60	430	
60	429	
60	428	
66	342	3.50.70.71.72.74
66	341	3.50.70.71.72.73.74
66	340	3.50.70.71.72.74
66	339	3.50.69.70.71.72.74
73	243	1.14.20
73	242	20
	50	24
	51	24
70.71	343	66
70.71	344	66
70.71	345	66
70.71	346	66
E	304	55.56.57
E	305	55.56.57
E	306	55.56.57
E	307	55.56.57
	402	56.58
	403	56.58
	404	56.58
	405	56.58.62
	406	58
	407	56.58
	408	56.58
	409	58



Circuit 64

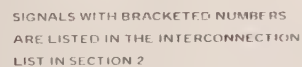
Interconnections		
Signal numbers are as in Section 2.4.		
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 64		
SOURCE	SIG No.	DESTINATION
54	52	56.57
58	577	
61	138	
58	322	
58	231	
32	348	69.71
32	347	69.71
34	416	
73	10	50
1	570	
56	19	
56	20	
58	70	
67	143	
67	142	
33	506	70
33	415	
33	487	
33	484	
33	483	
	71	58
54	120	56.57
54	119	56.57
54	118	56.57
	184	54
	492	58
70	327	66



64

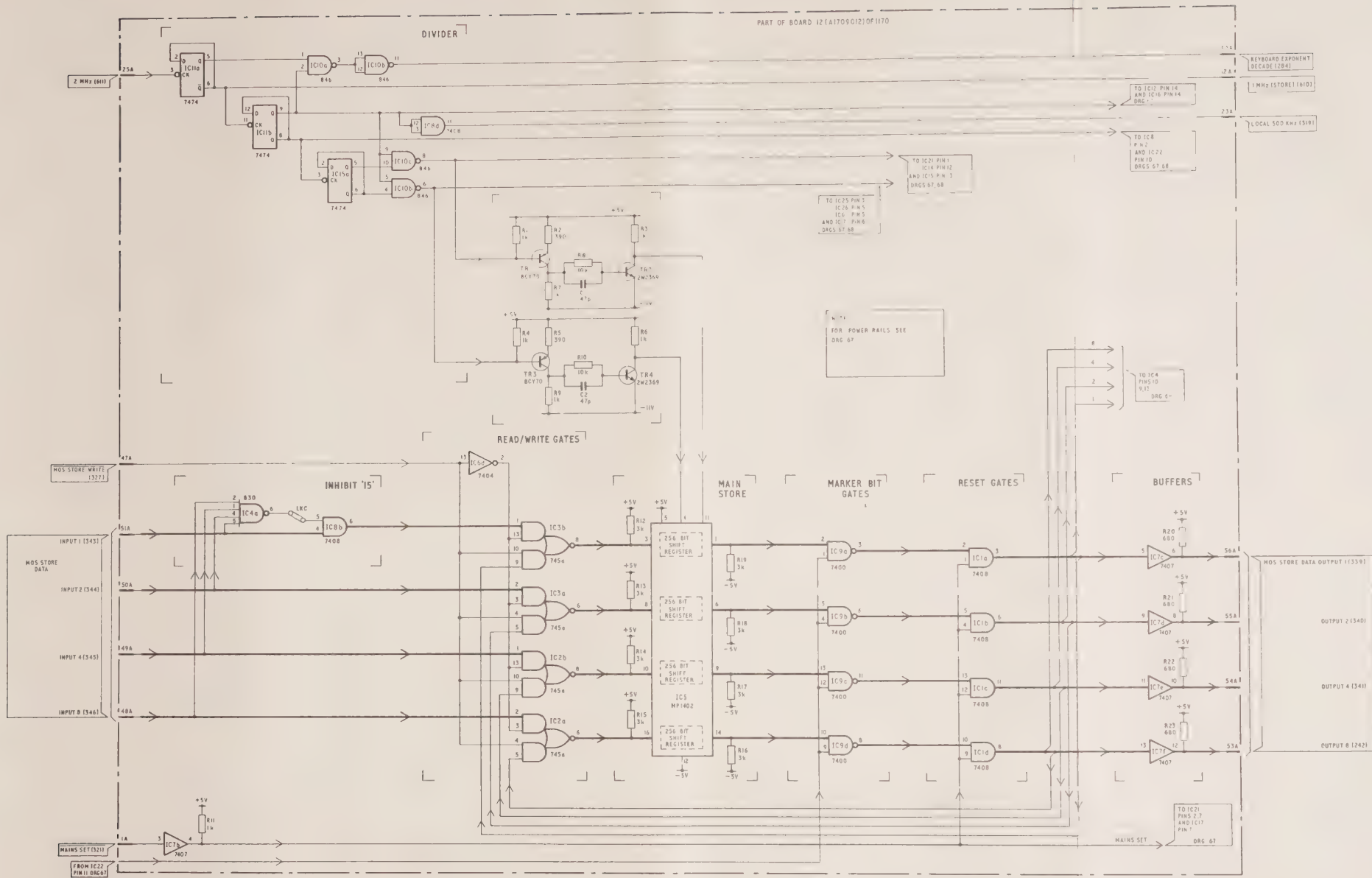
Circuit 65

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 65		
SOURCE	SIG No.	DESTINATION
58	230	
58	576	
61	491	
59	480	
59	481	
59	482	
59	479	
73	241	20
67	525	69
67	526	69
67	527	69
61	496	
67	522	69
61	495	
67	523	69
67	524	69
67	528	69
67	529	69
66	319	69
2	611	21.25.50.54.58.66.69.70.72
66	610	



Circuit 66

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 66		
SOURCE	SIG No.	DESTINATION
4	321	30.34.50.58
63.70.71	346	
63.70.71	345	
63.70.71	344	
63.70.71	343	
64.70	327	
2	611	21.25.50.54.58.65.69.70.72
70	284	71
65	610	
	319	65.69
	339	3.50.63.69.70.71.72.74
	340	3.50.63.70.71.72.74
	341	3.50.63.70.71.72.73.74
	342	3.50.63.70.71.72.74



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

MAIN STORE

66

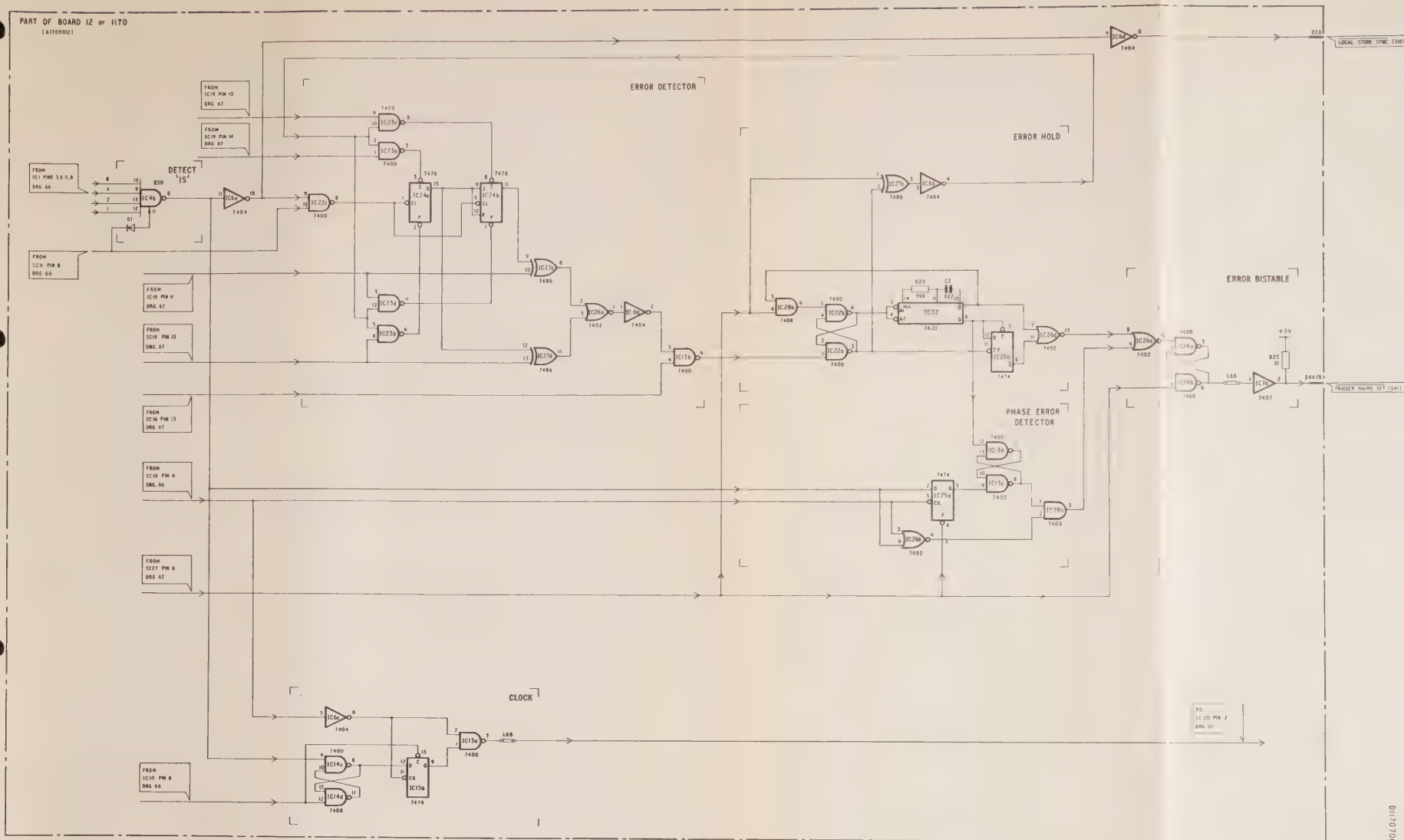
D1170/066 - 03

Circuit 67

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 67		
SOURCE	SIG No.	DESTINATION
70	166	71
70	140	
70	139	
70	554	
	522	65.69
	523	65.69
	524	65.69
	525	65.69
	526	65.69
	527	65.69
	528	65.69
	529	65.69
	542	3.69
	543	3.69
	538	69
	539	69
	540	69
	142	64
	143	64

Circuit 68

Interconnections Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 68		
SOURCE	SIG No.	DESTINATION
	318	69
	541	44



SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2

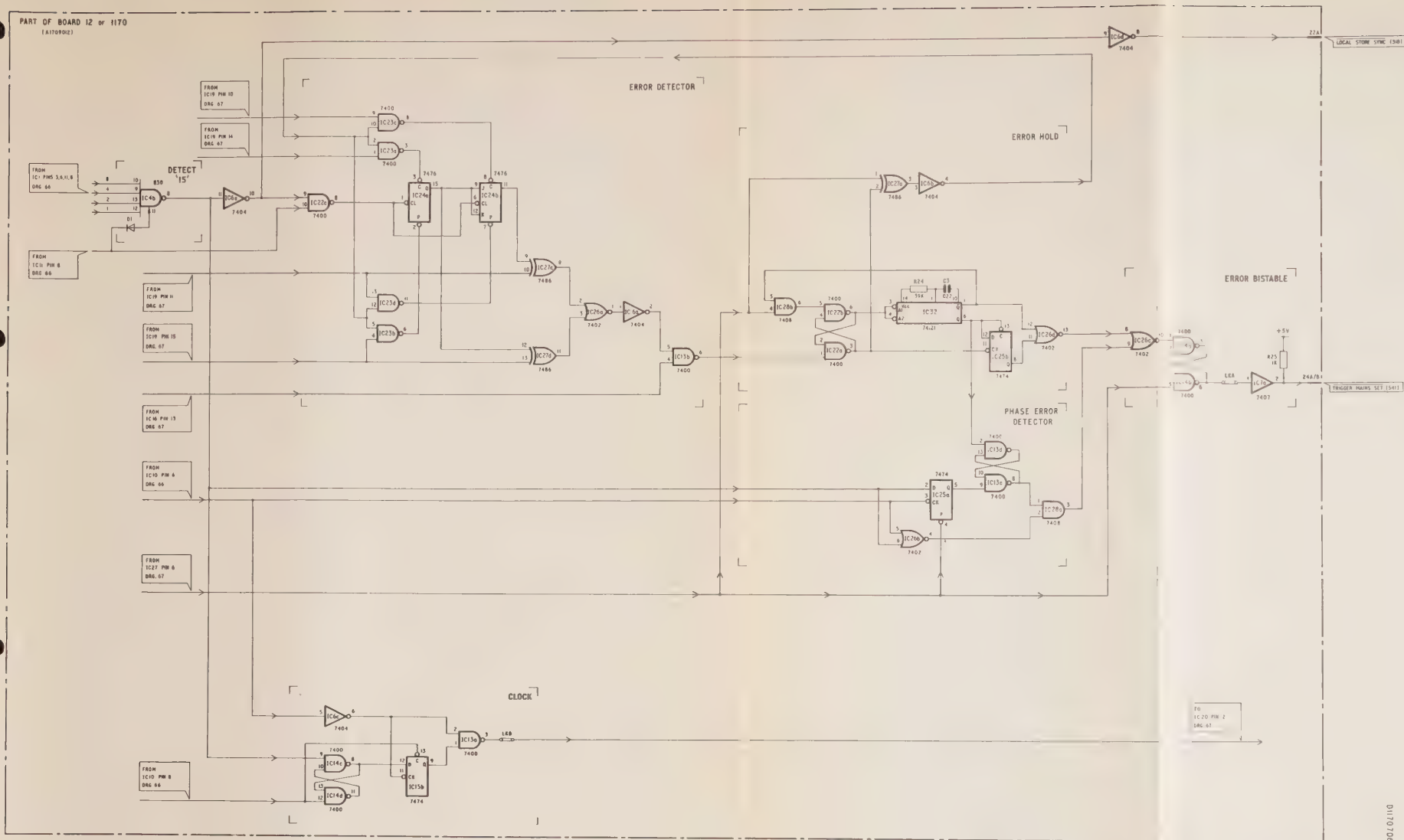
SOLUTION	DESIGN	USED ON	JOB STAGE	DEVELOPMENT ☒
	TEST			PRODUCTION
	EST		TITLE	ERROR
	DATE	CHANGA		DETECTION LOGIC
OT		SCALE	BOARD 12	
		DIMS		
		DRN	MAC	DATE 16 5 73
		CHD	DATE	
		APPD		
			D	DRAWING NUMBER
				11707068

ERROR DETECTION LOGIC BOARD 12

D11707068 - 02

Circuit 69

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 69			CIRCUIT No. 69 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
66	339	3.50.63.70.71.72.74		297	71.73
32	128	71.74		421	71
32	127	71		296	71
	412	74		169	50
32	347	64.71		100	72
32	348	64.71		490	70.72.74
67	542	3		94	72
67	543	3		530	31
67	522	65		99	72
67	523	65		531	31
67	524	65		95	72
67	525	65		532	31
67	526	65		90	72
67	527	65		533	31
67	528	65		93	72
67	529	65		534	31
68	318			535	31
66	319	65		536	31
67	540			537	31
67	539			608	30
67	538			170	3
2	611	21.25.50.54.58.65.66.70.72		358	3
70	277			295	74
70	278			420	74
70	279			13	3
70	280			417	23
70	281			546	70.71.72.75
70	282			545	70.71.72.75
70	283				
	183	70			
	273	70			
	92	72			



SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2

SOLUTION SEARCHED INDEXED SERIALIZED FILED	DATE	FILE	CHARGE	USED ON SCALE ☐ IN ☐ IN DRN MAC DATE 16 5 73 CHD DATE APPD	JOB STAGE ☐ DEVELOPMENT ☒ PRODUCTION
	OT				TITLE ERROR DETECTION LOGIC BOARD 12
					DRAWING NUMBER D 11707068

ERROR DETECTION LOGIC BOARD 12

D11707068 - 02

Circuit 70

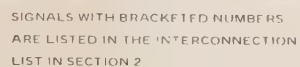
This circuit controls the display of data commanded from the Keyboard (the extreme right-hand display) and the entry of the data into the MOS store.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 70			CIRCUIT No. 70 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
33	506	64		139	67.71
36.71	276			265	75
36.71	275			266	75
36.71	274			267	75
69	490	72.74		268	75
69	273		63.71	343	66
36	287	70.71	63.71	344	66
31	212	36.71	63.71	345	66
36.71	485		63.71	346	66
62	68			264	71
2	611	21.25.50.54.58.65.66.69.72	64	327	66
69	183			410	71
31	592			146	71
31	591			140	67
66	342	3.50.63.71.72.74	66	284	71
66	341	3.50.63.71.72.73.74		283	69
66	340	3.50.63.71.72.74		282	69
66	339	3.50.63.69.71.72.74		278	69
69	545	71.72.75		281	69
69	546	71.72.75		280	69
31	259	73		279	69
31	258	36.71.73		166	67
31	286			285	71
31	257	36.71.73		554	67
31	256	36.71.73		277	69
	121	71		411	71
	65	71		141	71
	410	71			

Circuit 71

This circuit controls the display of data commanded from the Keyboard (the extreme right-hand display) and the entry of the data into the MOS store.

Interconnections			Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.			Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 71			CIRCUIT No. 71 (cont.)		
SOURCE	SIG No.	DESTINATION	SOURCE	SIG No.	DESTINATION
36	288		69	296	
31	212	36.70	32	127	69
33	313	36	32	348	64.69
36	287		32	347	64.69
31	258	36.70.73		298	74
31	257	36.70.73		299	74
31	256	36.70.73		300	74
32	128	69.74		301	74
69	297	73		553	74
69	421			328	74
66.70	284			330	74
70	411			213	74
70	141			289	74
70	264			269	75
70	121			270	75
	618			271	75
35	172			272	75
35	171		63.70	343	66
70	146		63.70	344	66
35	173		63.70	345	66
70	65		63.70	346	66
70	285		36	274	70
66	342	3.50.63.70.72.74	36	275	70
66	341	3.50.63.70.72.73.74	36	276	70
66	340	3.50.63.70.72.74	36	485	70
66	339	3.50.63.69.70.72.74	36.73	290	37
70	139	67	36.73	291	37
72	252		36.73	292	37
70	410				
62	69				
69	546	70.72.75			
69	545	70.72.75			

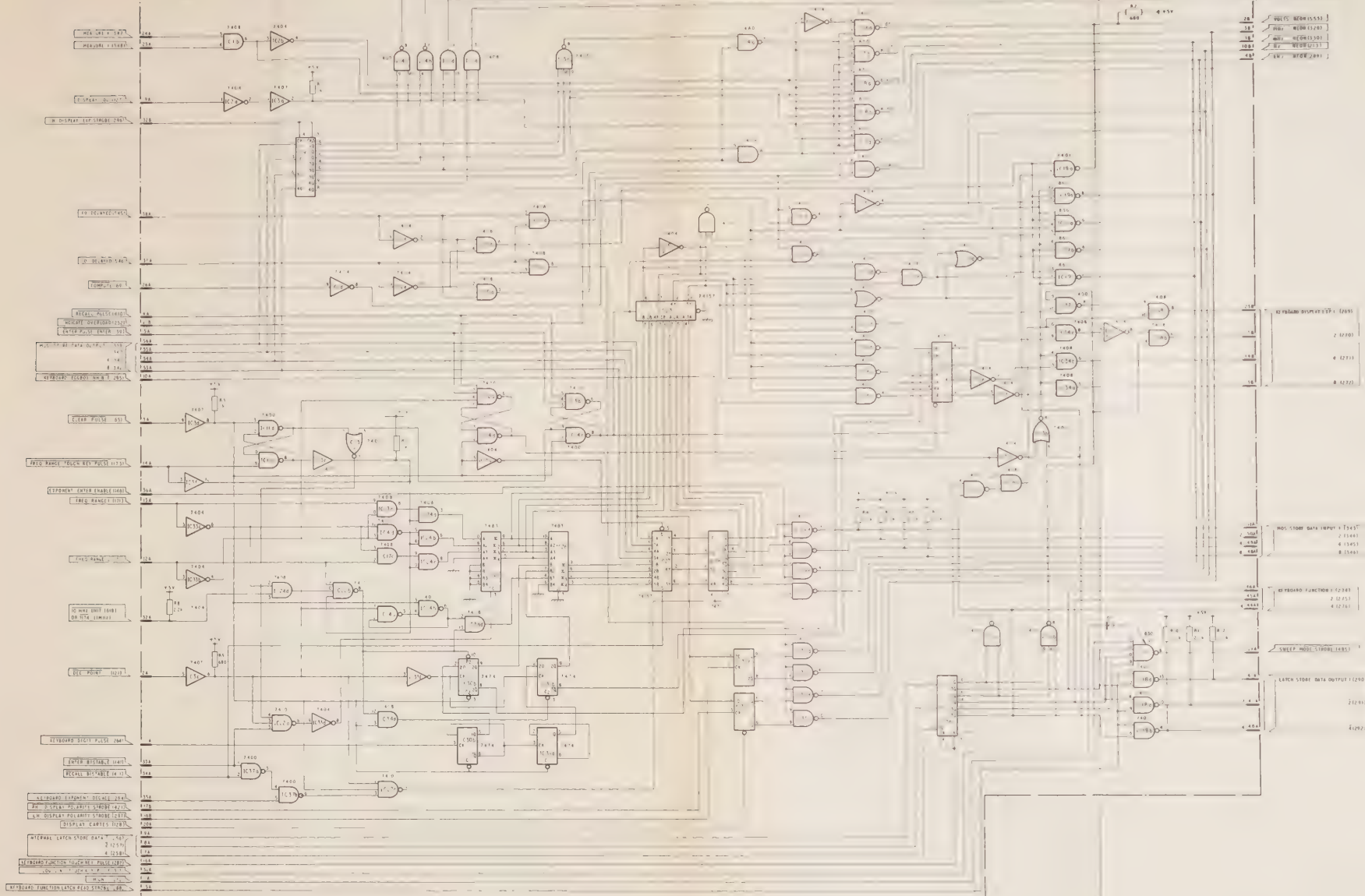


Circuit 72

This circuit generates the D/A mark/space pulse trains, the use of which is described in "Introduction to the Generator".

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 72		
SOURCE	SIG No.	DESTINATION
66	342	3.50.63.70.71.74.
66	341	3.50.63.70.71.73.74.
66	340	3.50.63.70.71.74.
66	339	3.50.63.69.70.71.74.
69	92	
69	490	70.74.
69	546	70.71.75.
69	545	70.71.75.
46.48	632	74.75
2	611	21.25.50.54.58.65.66.69.70.
69	95	
69	94	
69	93	
69	100	
69	90	
69	99	
	451	4
	450	
	455	22
	456	22
	101	
	102	
	103	
	425	22
	426	22
	91	4
	96	
	174	25.30
	414	22
	419	22
	187	4
	186	4

BOARD 16 OF 170
(A1709016)



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

DISPLAY DECODE

71

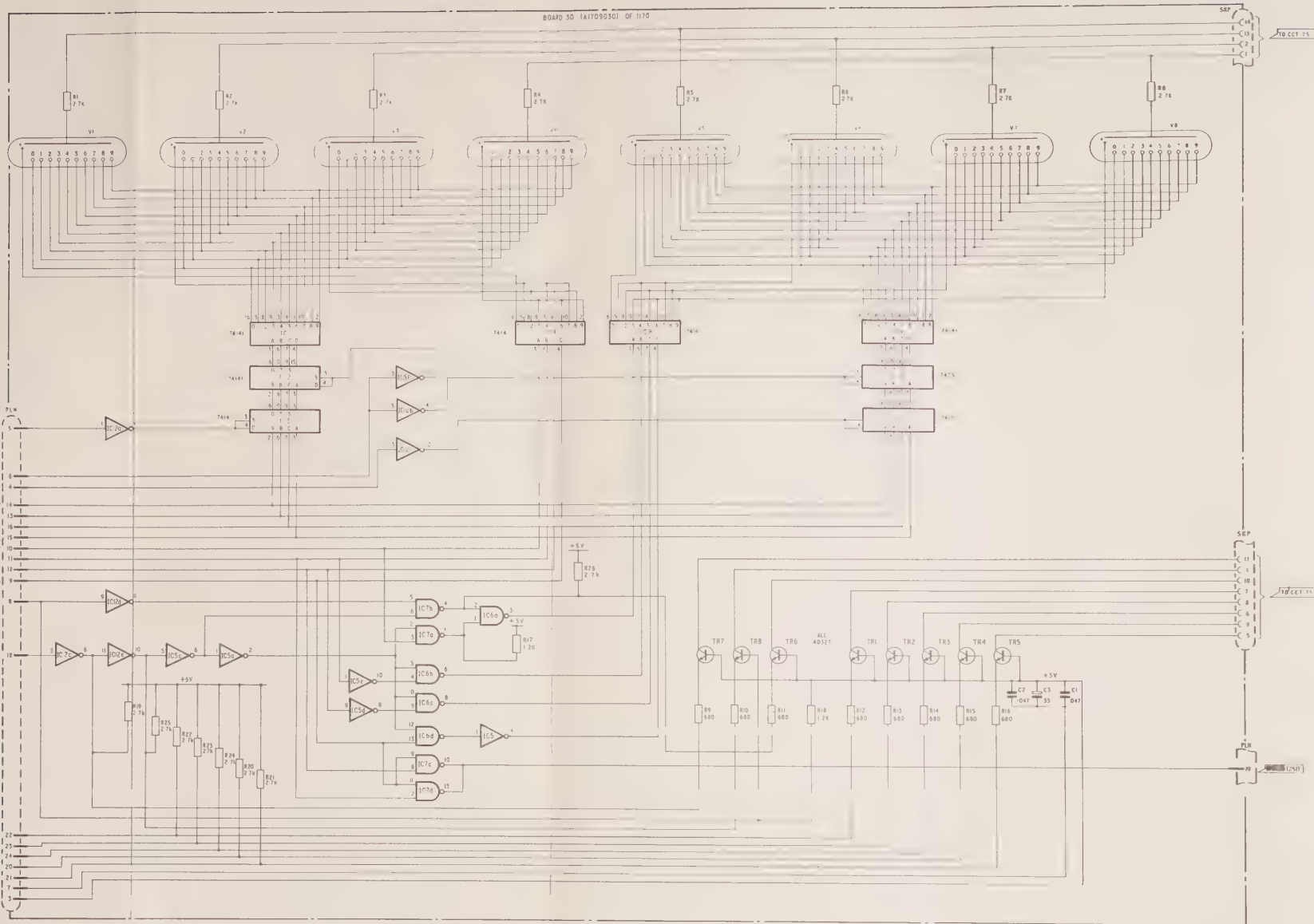
D11707071 - 04

Circuit 73

This circuit controls the Auto ranging and overload indicator system.

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 73		
SOURCE	SIG No.	DESTINATION
69	297	71
66	341	3.50.63.70.71.72.74.
33	122	
2	598	
62	424	
14.21	260	
62	427	
62	232	
31	17	
31	259	70
31	258	36.70.71.
31	257	36.70.71.
31	256	36.70.71.
62	438	29.33.
31	253	
31	240	
31	355	
36.71	290	37
36.71	291	37
36.71	292	37
	293	37
	241	20.65
	242	20.63
	243	1.14.20.63
	10	50.64
	312	56
	252	71





SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 74

Interconnections

Signal numbers are as in Section 2.4.

Sources and destinations are circuit diagram numbers;
if none shown all connections are within this circuit.

CIRCUIT No. 74

SOURCE	SIG No.	DESTINATION
46	632	72.75
71	553	
71	330	
71	213	
71	289	
71	328	
32	128	69.71.
	412	69
71	301	
71	300	
71	299	
71	298	
66	342	3.50.63.70.71.72.
66	341	3.50.63.70.71.72.73.
66	340	3.50.63.70.71.72.
66	339	3.50.63.69.70.71.72.
69	420	
69	490	70.72
69	295	
34	251	75

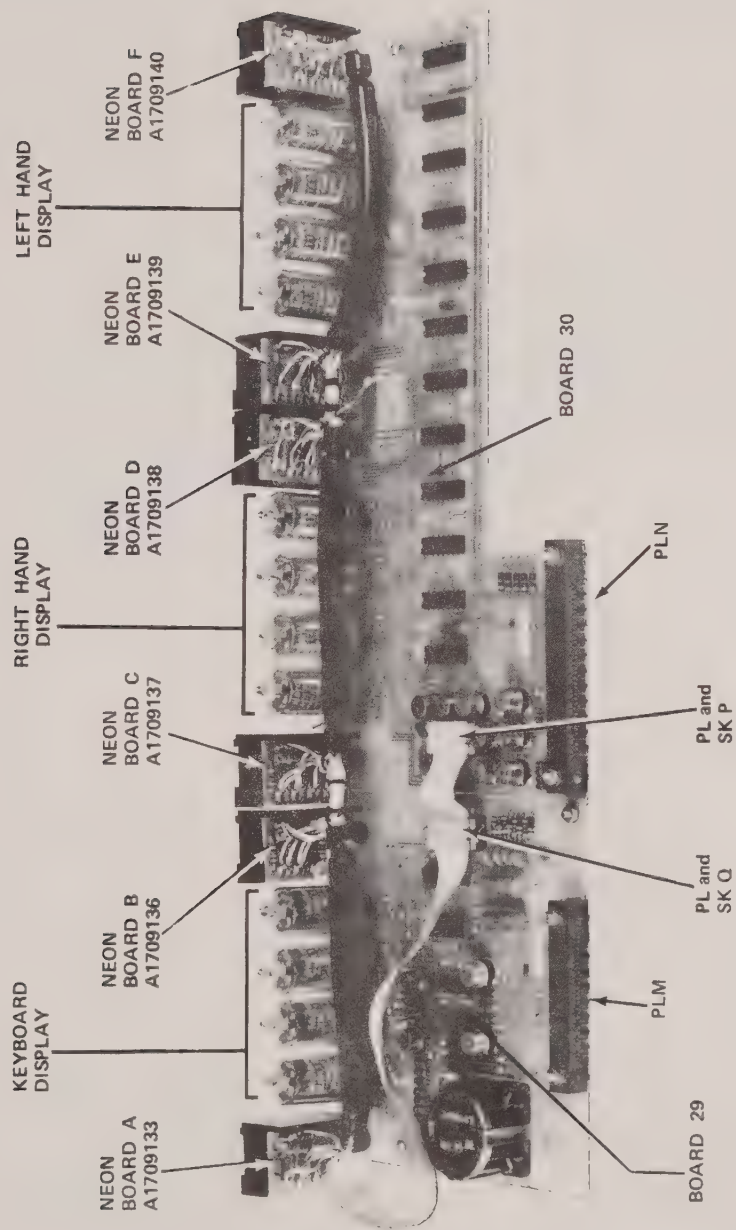
The Display Unit Circuits 74 and 75

This is a detachable assembly consisting of pcbs 29, 30 and Neon boards A to F.

The display consists of three banks of four numerical indicator tubes and six stacks of Neon lamps (Eggboxes).

All indicators are supplied from a 160V inverter and carried on four time-shared lines. The inverter consists of TR4, TR5 and associated circuitry. Time-sharing of the four lines is controlled by input lines T9 and T10 delayed (545, 546).

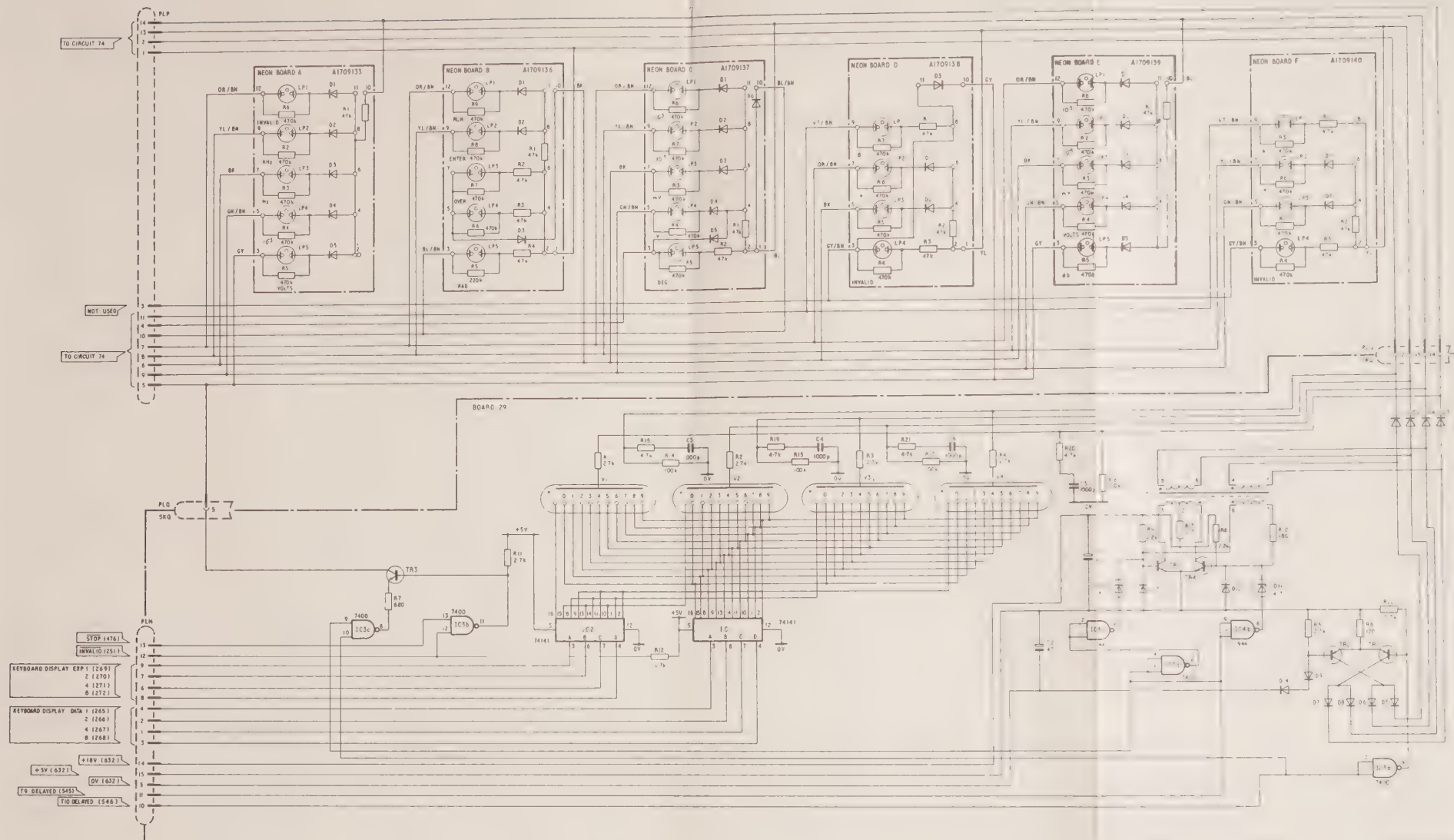
The rest of the circuitry of the display unit is used to decode the signals from the digital section. The required combination of high voltage on the diode and zero on the cathode illuminates the correct combinations of indicators. As this is a time-shared operation only certain combinations of indicators may be illuminated at a time. The sequential and repetative scanning of the correct indications form the apparently steady display.



DISPLAY ASSEMBLY CIRCUIT 75

Circuit 75

Interconnections		
Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 75		
SOURCE	SIG No.	DESTINATION
69	546	70.71.72.
69	545	70.71.72.
46.47.48	632	72.74.
70	268	
70	267	
70	266	
70	265	
71	272	
71	271	
71	270	
71	269	
34.74	251	
33	476	50



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

DISPLAY ASSY (2)

75

D11707075 - 03A

APPENDIX B2 – STORE STATE INDICATOR

TG 1212A Store State Indicator

A 256 bit pulse train generated from the 2MHz, 500kHz and Sync. inputs synchronises with the clock used for the MOS and Latch stores. This pulse train is used to generate strobes which determine the store time-slot selected.

Read

The Sync. pulse starts a pulse train and loads into IC3 and 4 a number selected on the store address switches and a number (0 - 7) from IC12.

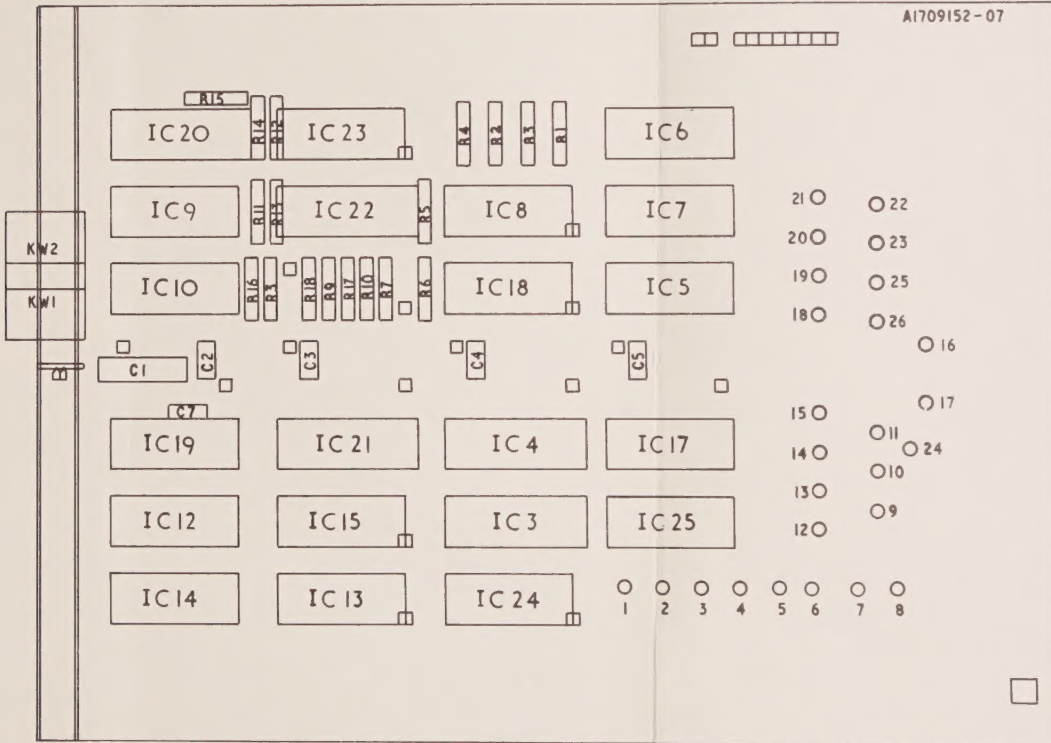
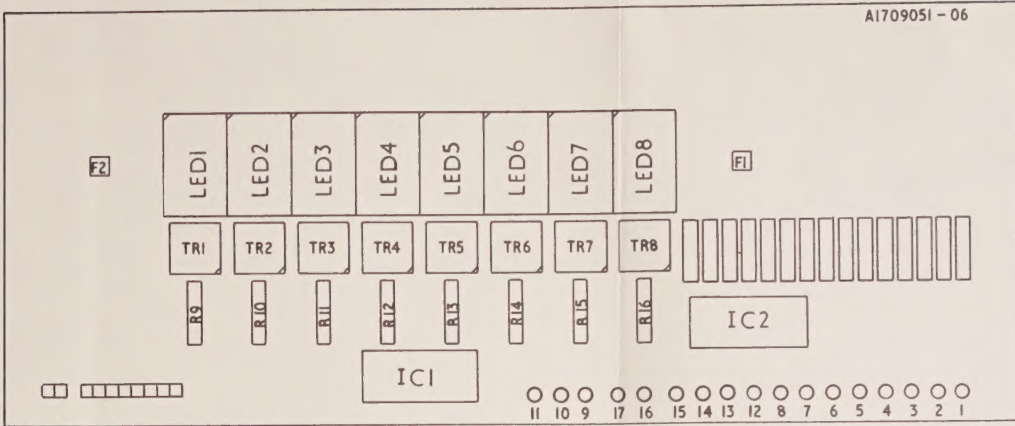
IC3 and 4 then count down at 500kHz until they are empty, when a pulse is passed to IC22. Data on the output busses (MOS or Latch depending on IC20) will be latched into IC21. These data will be displayed, after the next Sync pulse, on the LED selected by IC12 (which also selected the decade address) and IC1.

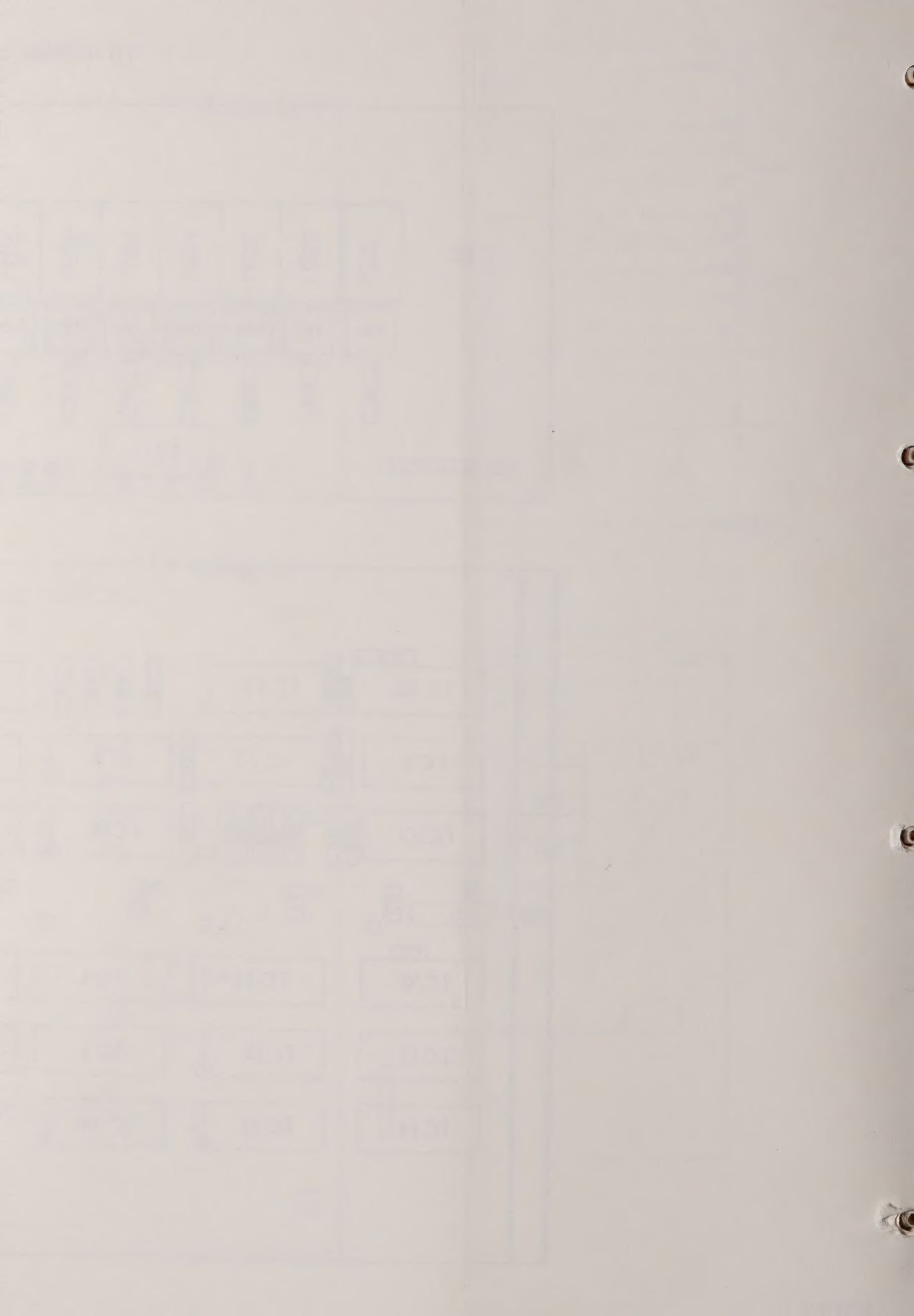
The following pulse train will repeat the action, the decade address having stepped on one count and hence selecting the next store location and LED. The action will repeatedly step through the eight locations of the selected MOS store address, or the two of the Latch store.

Write

Pressing the write button causes bistable IC6 to flip over at the next Sync pulse. The selections of all three octal switches are loaded into IC3 and 4. When the contents of IC3 and 4 reaches zero a write strobe is generated via IC5, 7 and 8 and EC35 and 47A. This will cause the data on the input busses from the data switches to be written into the selected location via IC9 or 10 depending on which is selected.

COMPONENT LAYOUT 1170 PCB's 51 & 52





SOLARTRON

Schlumberger

THE SOLARTRON ELECTRONIC GROUP LIMITED
FARNBOROUGH HAMPSHIRE ENGLAND GU14 7PW TEL. FARNBOROUGH 44433 (STD 0252)
CABLES: SOLARTRON FARNBOROUGH HANTS. TELEX: 858245 SOLARTRON FARNBOROUGH